IEEE Rebooting Computing Summit 4 (RCS 4)

Roadmapping the Future of Computing:
Discovering How We May Compute

9-11 December 2015, Washington Hilton, Washington DC
Follows the end of International Electronic Devices Meeting (IEDM 2015)

RCS 4 is by invitation only, but spots for qualified attendees may still be available. Please contact Bichlien Hoang (b.hoang@ieee.org) if you are interested in attending.

IEEE 2015 RCS 4 Co-Chairs
Erik DeBenedictis, IEEE Computer Society and Sandia National Laboratory
David Mountain, IEEE Electron Device Society and National Security Agency

IEEE Rebooting Computing Initiative Co-Chairs
Tom Conte, Ph.D - President, IEEE Computer Society
Elie Track, Ph.D - Past President, IEEE Council on Superconductivity

Rebooting Computing Summit 4 – Preliminary agenda as of Nov 23, 2015

Workshop activities start 6 PM Wednesday November 9 with a reception. The workshop is at the same hotel as the IEDM conference (Washington Hilton) and begins about the time IEDM ends.

The first full day Thursday begins at 8:30 AM with an overview of the Rebooting Computing initiative, followed by summary presentations by other organizations with initiatives in the field, including ITRS 2.0, SRC, NSCI, and the OSTP Grand Challenge.

A principal purpose of the workshop is to establish an understanding amongst participants of timescales for the development and emergence of new approaches to computing. These timescales are expected to become the basis of new computer-level road mapping that should succeed the Moore's Law-type semiconductor road mapping that has been in place for around 15 years. The workshop will feature leading approaches to computing based on various measures of effectiveness, such as performance, power efficiency, and/or utility. The first three approaches will be described by a visionary presentation followed by one of experimental results, with a fourth approach described in a single presentation. All presentations will be accompanied by a peer-reviewed academic paper in the December issue of IEEE Computer magazine (provided to participants). The four technology tracks are:

(1) Brain-inspired computing, focusing on the OSTP nano-inspired Grand Challenge. The particular form of brain-inspired computing will be computer systems that process "Big Data" and also learn from the data using methods from the brain (it is not artificial intelligence or building a brain).

(2) A class of computing methods known as stochastic, probabilistic, and approximate computing. As the power consumption of computer components goes down, the reliability goes down as well. The rise in error can be accommodated in various ways, which will be described.

(3) 3D integration and new low power devices, which is essentially the continuation of Moore's Law through new disruptive devices and manufacturing technology.

(4) Superconducting electronics, an approach of using the Josephson Junction in lieu of the transistor while preserving existing architectures and retaining software compatibility with today's codes.

After a review of additional initiatives (DARPA and IARPA), participants will divide into three tracks whose objective is to formulate realistic expectations and timeframes for each of the three technology areas. The tracks will include specialists in the various areas and may include some talks. However, the working group objectives will be to establish a very rough road map for each of the areas.

Friday likewise begins at 8:30 with a review and then continuation of the working groups, also including specialists and additional presentations as needed. The second working group sessions will debrief before lunch.

The workshop will formally conclude at 12:30 PM Friday, yet the IEEE/RC "Sensible Machine" activity will have a group meeting during Friday afternoon. Information on the Sensible Machine activity will be available elsewhere.

Wednesday, December 9, 2015			
6:00 PM	Reception		
9:00 PM	End reception		
Thursday, December 10, 2015			
8:30 AM	Review of impetus for IEEE RC initiative, review of RC summits (3 pillars, complementary nature of various approaches, etc.). Tom Conte/Elie Track		
8:45 AM	Review of other initiatives in this area – ITRS 2.0 Paolo Gargini		
9:00 AM	Review of other initiatives in this area – SRC William Joyner		
9:15 AM	Review of other initiatives in this area – NSCI William Koella		
9:30 AM	Review of other initiatives in this area – OSTP Grand Challenge Lloyd Whitman		
9:45 AM	Roadmapping the future of computing TBD		
10:00 AM	Break		
10:30 AM	Tech 1: Neuromorphic/Sensible Machine big picture and experimental results Stan Williams; Dave Mountain		
11:45 AM	Tech 2: Probabalistic/random/approximate big picture and experimental results L. Monroe; S. Khasanvis (tent.)		
1:00 PM	Lunch		
2:00 PM	Tech 3: 3D integration and new devices big picture and experimental results Kirk Bresniker; H. S. Philip Wong		
3:15 PM	Tech 4: Superconductive electronics/C^3 Marc Manheimer		
3:45 PM	Break		
4:15 PM	Review of other initiatives in this area – DARPA Dan Hammerstrom		
4:30 PM	Review of other initiatives in this area – IARPA Jason Matheny		
4:45 PM	Tech 1: Brain-Inspired	Tech 2: Probabalistic	Tech 3: More Moore
	Learning devices TBD	TBD TBD	Improved transistors TBD
	Nonlinear dynamics TBD	TBD TBD	Roadmap structure TBD
6:00 PM	Posters		
7:00 PM	Reception starts in poster area		
Friday, December 11, 2015			
8:30 AM	First working group review		
9:00 AM	Tech 1: Brain-Inspired	Tech 2: Probabalistic	Tech 3: More Moore
	TBD TBD	TBD TBD	TBD TBD
11:00 AM	Second working group review		
12:00 PM	Lunch		
12:30 PM	RCS 4 Adjourns		
1:30 PM	Associated IEEE/RC "Sensible Machine" Grand Challenge group meeting		
6:00 PM	Sensible Machine group meeting adjourns		