Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

Rebooting Computing: SRC Related Efforts

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SRC: A Family of Distinct, Related Programs

Global Research Collaboration

Ensuring vitality of current industry

STARnet

Early research engagement of long horizon semiconductor challenges

Nanoelectronics Research Initiative

Beyond CMOS – the next switch and associated architectures

Education Alliance

Attracting and educating the next generation of innovators and technology leaders

- Nonpofit member-driven research consortium
- Has supported >$2B in research at >250 universities

Member Based, Member Driven

SRC GRC Thrust Topics

- Trustworthy and secure semiconductors and systems
- Internet of Things
- Energy efficiency (and performance) in computing
- Convergence of biology and microelectronics
- Analog/Mixed-Signal Circuits, Systems, Devices
- System Level Design
- Logic and Memory Devices
- CAD and Test
- Packaging
- Environment, safety, and health
- Nanomanufacturing
- Cross-disciplinary (SRC's exploratory research grant program)

More information about each thrust can be found at https://www.src.org/program/grc/ (see listing on left-hand side).

Rebooting Computing: SRC Efforts

- Rebooting the IT Revolution
- SemiSynBio Roadmap Initiative with NIST
- Efficiency and Performance for Connectivity Constrained Computing (EP3C)
- Trustworthy and Secure Semiconductors and Systems (T3S/STARSS) Joint Program with NSF

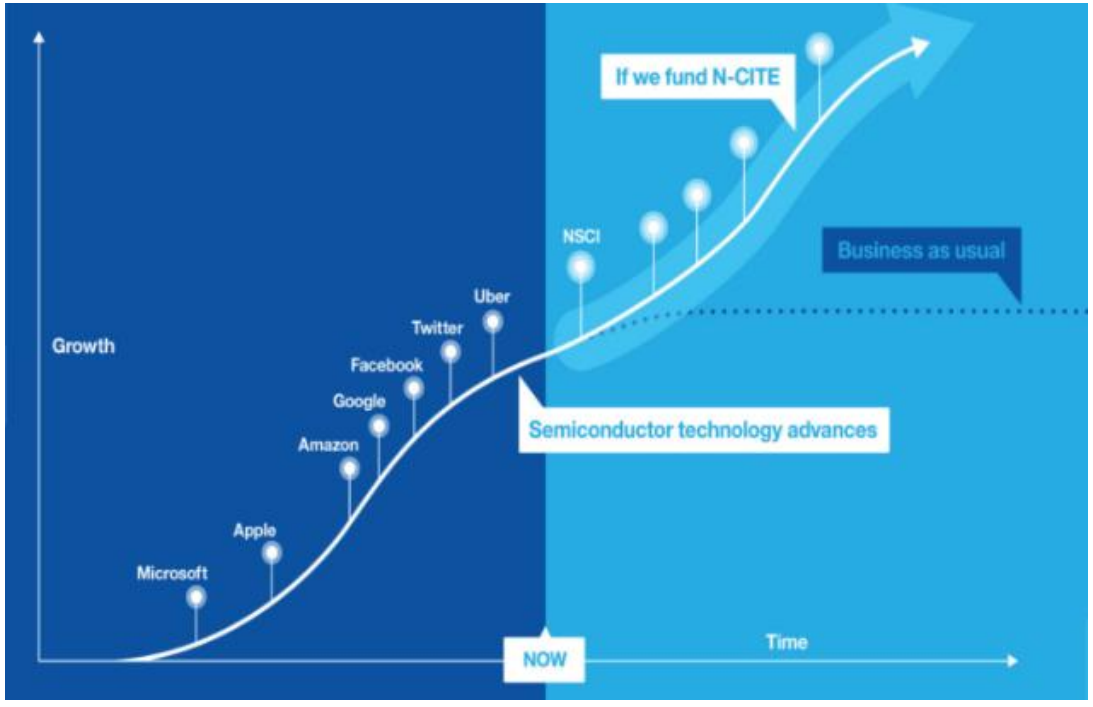
Rebooting the IT Revolution: A Call to Action

- **March 2015:** NSF Workshop sponsored by SIA and SRC

- **September 2015:** Report identifying "fundamental research needs for advancing the burgeoning IoT and catalyzing cutting-edge innovations that will support future US technology leadership and economic competitiveness." https://www.src.org/newsroom/rebooting-the-it-revolution.pdf

"Rebooting" Workshop and Report

- Positive Reaction from Research Agencies
  - White House announced nanotechnology-inspired Grand Challenge for Future Computing that relied heavily on the report: *"Create a new type of computer that can proactively interpret and learn from data, solve unfamiliar problems using what it has learned, and operate with the energy efficiency of the human brain."*
  - From NSF: After receiving 100+ responses to the Grand Challenge RFI, "the workshop on Rebooting IT was the most relevant precursor" to the Grand Challenge selection.
- Follow-on workshop being planned for April



Celia Merzbacher
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"Rebooting" Research Challenges

Energy Efficient Sensing and Computing
Development of novel materials, devices, or architectures to reduce power consumption

Cyber-Physical Systems
New systems based on computational algorithms and physical components that transform the way people interact with engineered systems

Intelligent Storage
New memory technologies and management systems to store and archive the explosion of projected data

Real-Time Communication Ecosystem
Research in communication network architectures to transmit and receive data quickly for analysis, while minimizing energy utilization and transmission errors

Multi-Level and Scalable Security
Development of new sensors, computing and communications technology that can increase security for IoT and other applications

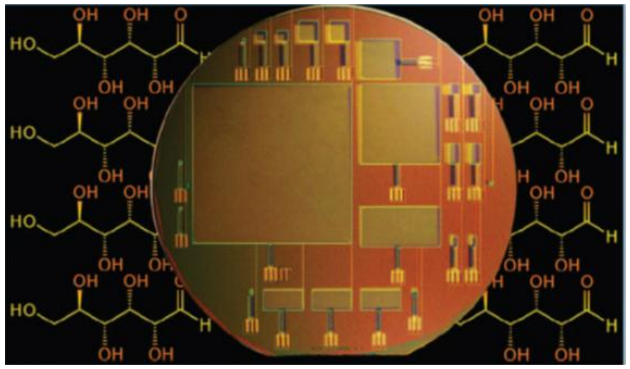
Next Generation Manufacturing
Fundamental research on materials, fabrication, assembly, and packaging to support fabrication of future chips

Next Insight Computing
Research on new computing capabilities to extract actionable intelligence from raw data

IoT Test Platform
Development of the infrastructure to test new technologies with solution verification and benchmarking

Semiconductor Synthetic Biology (SemiSynBio)

- **Goal:** New solutions for the semiconductor and IT industries
- **2013:** SRC launched an *exploratory research program* in SemiSynBio with efforts directed toward projects with five-to-ten year impact on semiconductor technologies
- **2015:** SRC and NIST with support from member companies launched the *SemiSynBio Roadmap initiative*



Selected SemiSynBio Topics

- DNA-based massive information storage
  - Great potential as future-generation storage technology
    - In theory, one kilogram of DNA has a storage capacity of ~10^{24} bit, which is equivalent to the total projected world's storage requirement in 2035-2040.
    - For comparison, to store ~10^{24} bit in flash requires ~10^{9} kg of wafer-grade Si (estimated global supply of wafer-grade Si is ~ 10^{7} kg in 2040)
- Lessons from biology on computational models and computer architectures
  - Computational models derived from cell biology
  - Cell-inspired and cell-based physical and computational systems
    - Focus on minimum energy systems
- Hybrid semiconductor-biological systems
  - Live cell-microelectronic systems for next-generation sensing functionalities

SemiSynBio Consortium and Roadmap Development

- SRC and NIST with support from member companies launched the SemiSynBio Roadmap initiative
  - Award from NIST Advanced Manufacturing Program
  - 30 participating organizations from industry, government, academia
    - Autodesk, Micron, Microsoft, Raytheon BBN, Intel, IBM, Mentor Graphics, GLOBALFOUNDRIES, Twist Biosciences, Gingko Bioworks, SynBioBeta, . . .
    - Columbia, Dartmouth, Georgia Tech, NC State, UCLA, Illinois, . . .
    - DoD, NIST, NSF, . . .
- The Roadmap will identify technology targets/goals, challenges and barriers to advanced manufacturing, and define quantitative metrics of progress in:
  - DNA-based Massive Information Storage
  - Energy Efficient, Small Scale Cell-inspired Communication Systems
  - Intelligent Sensor Systems
  - Biological System Design Automation
  - DNA-controlled Sub-10 nm Manufacturing

SemiSynBio

- Exploration of synergies between semiconductor technology and synthetic biology is a promising research topic
  - game-changing and long-term
  - early engagement by industry could provide significant downstream business opportunities

- More participants are welcome!
  Victor Zhirnov (victor.zhirnov@src.org)

EP3C/E2CDA
Energy Efficient Computing from Devices to Architectures

- **Goal:** Create the next paradigm of 'general purpose computing' for applications from mobile devices to data centers
- **Characteristics:**
  - Orders of magnitude higher levels of *computational energy efficiency*
  - Substantially increased *system-level functional density*
  - *Workflow-adaptive and scalable* platform to address the broadest range of applications from the edge to the core
  - Neuro-inspired *cognitive learning and predictability*, integrated on the same physical platform with ultra-efficient arithmetic computation
  - *Co-optimization* of materials and devices-to-system architecture by cross-disciplinary, collaborative research teams all guided by a common set of system-level, workflow requirements

EP3C
Thrust Areas

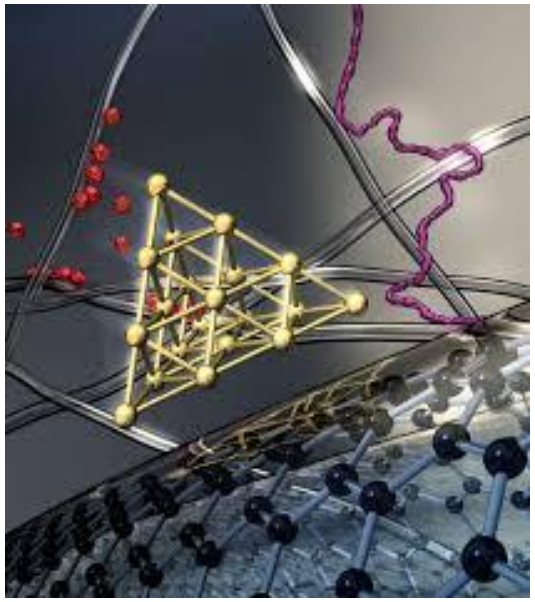
- **Revolutionary hybrid architectures** with programmed arithmetic logic integrated on the same physical platform with neuro-inspired adaptive learning and predictive capabilities

- **Revolutionary device concepts** and associated circuits and architectures that greatly extend the practical engineering limits of energy efficient computing

- **Novel materials for '1-D' on-chip conductors** with substantially reduced parasitics and potentially, embedded 'routing intelligence'

EP3C Program

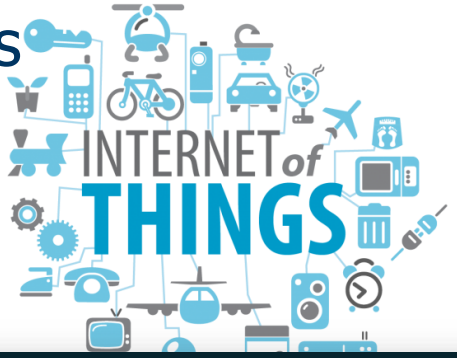
- SRC 'seed program' launched December 2015
- Discussion with NSF about joint effort involving SRC's GRC and NRI
- April 2015 report: www.src.org/program/grc/ep3c/



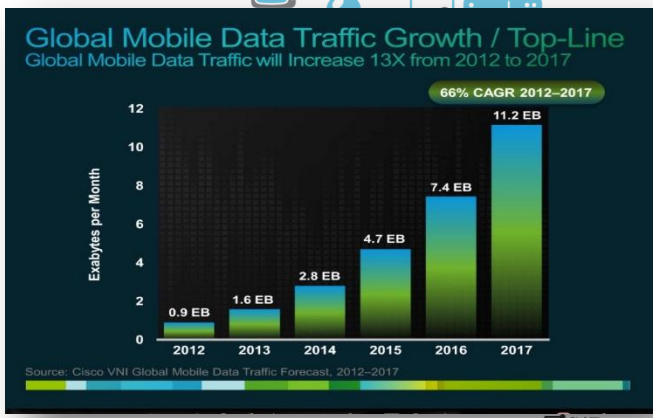
- Jon Candelaria (jon.candelaria@src.org)

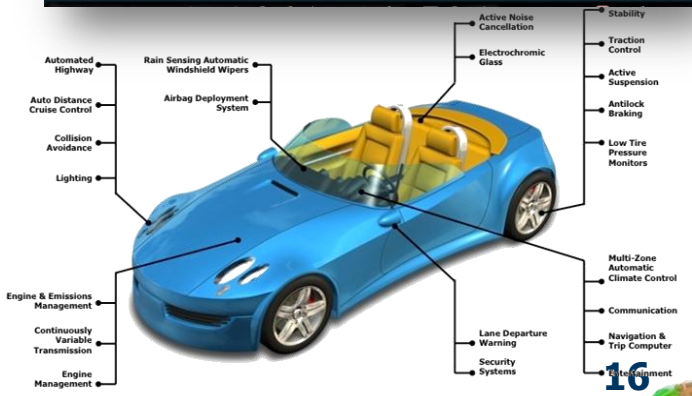
T3S (Trustworthy and Secure Semiconductors and Systems)

- **Goal:** Develop cost-effective strategies and tools to design and manufacture chips and systems that are reliable, trustworthy, secure and resistant to attack or counterfeiting.



- Drivers: Semiconductors and systems are
  - More pervasive and embedded
  - More complex
  - More dependent on 3rd party IP
  - More reliant on global supply chain
  - More networked
  - More vulnerable
  - More critical if they fail
  - More attractive to adversaries





Source: ChipEstimate.com

T3S (Trustworthy and Secure Semiconductors and Systems)

- Three-phase $10M joint program with National Science Foundation
- 25 ongoing projects – more to be selected in 2016
- Current areas of research:
  - Counterfeit Detection and Avoidance
  - Security by Design
  - Verification
  - Attack Aware

T3S (Trustworthy and Secure Semiconductors and Systems)

- Summary: Provide maximum assurance that IP/chips/ systems perform only as intended without impacting time to market, cost and performance and are resistant to attack/theft
- Objectives:
  - Develop cost-effective strategies, techniques and tools to increase security, trust, and assurance in products. Potential industry driven activities include development of
  - Partner with government to leverage investment
  - Grow/tap into the university research enterprise
  - Participate in defining the security agenda
  - "Get in front of the threat."

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Thank You!