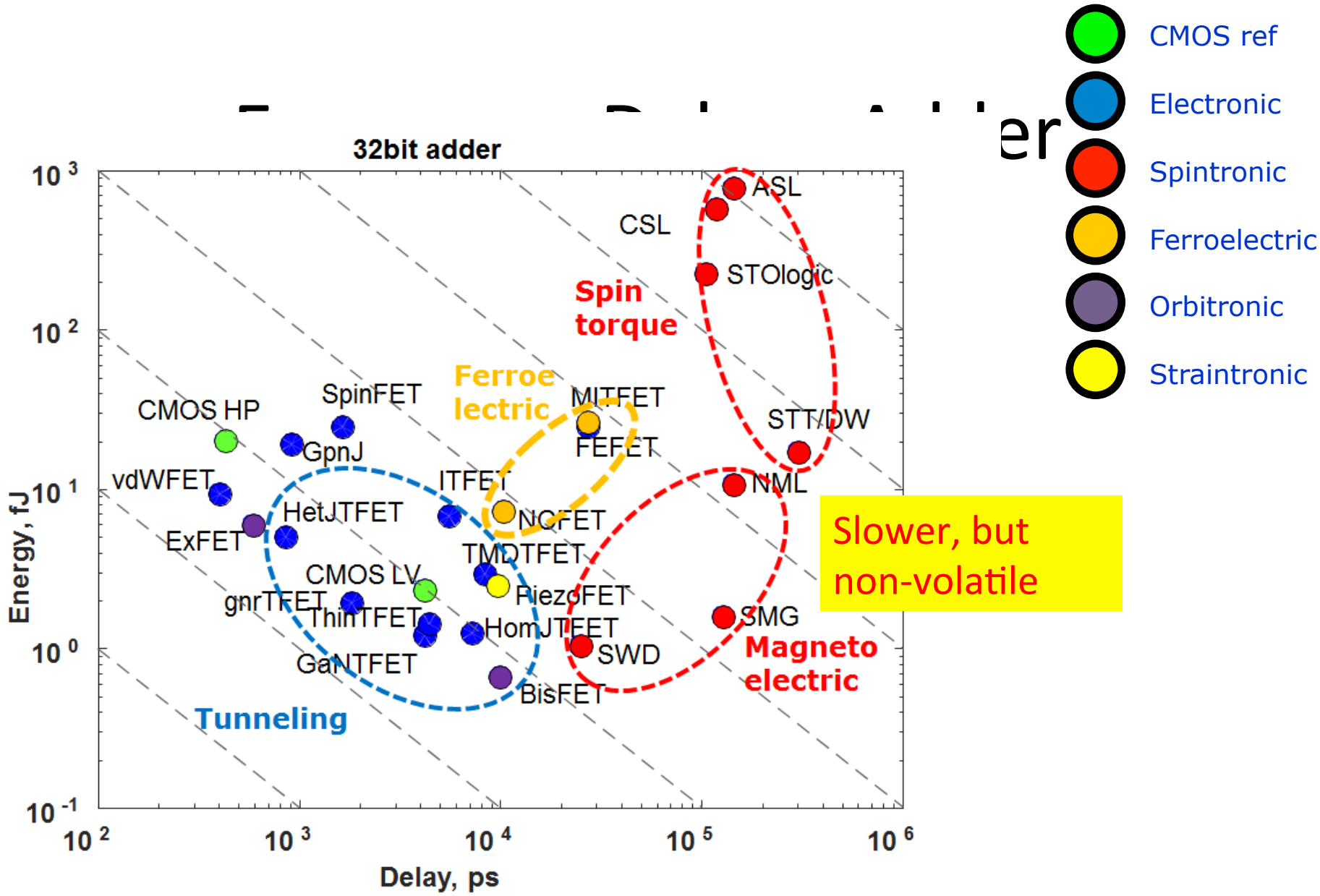
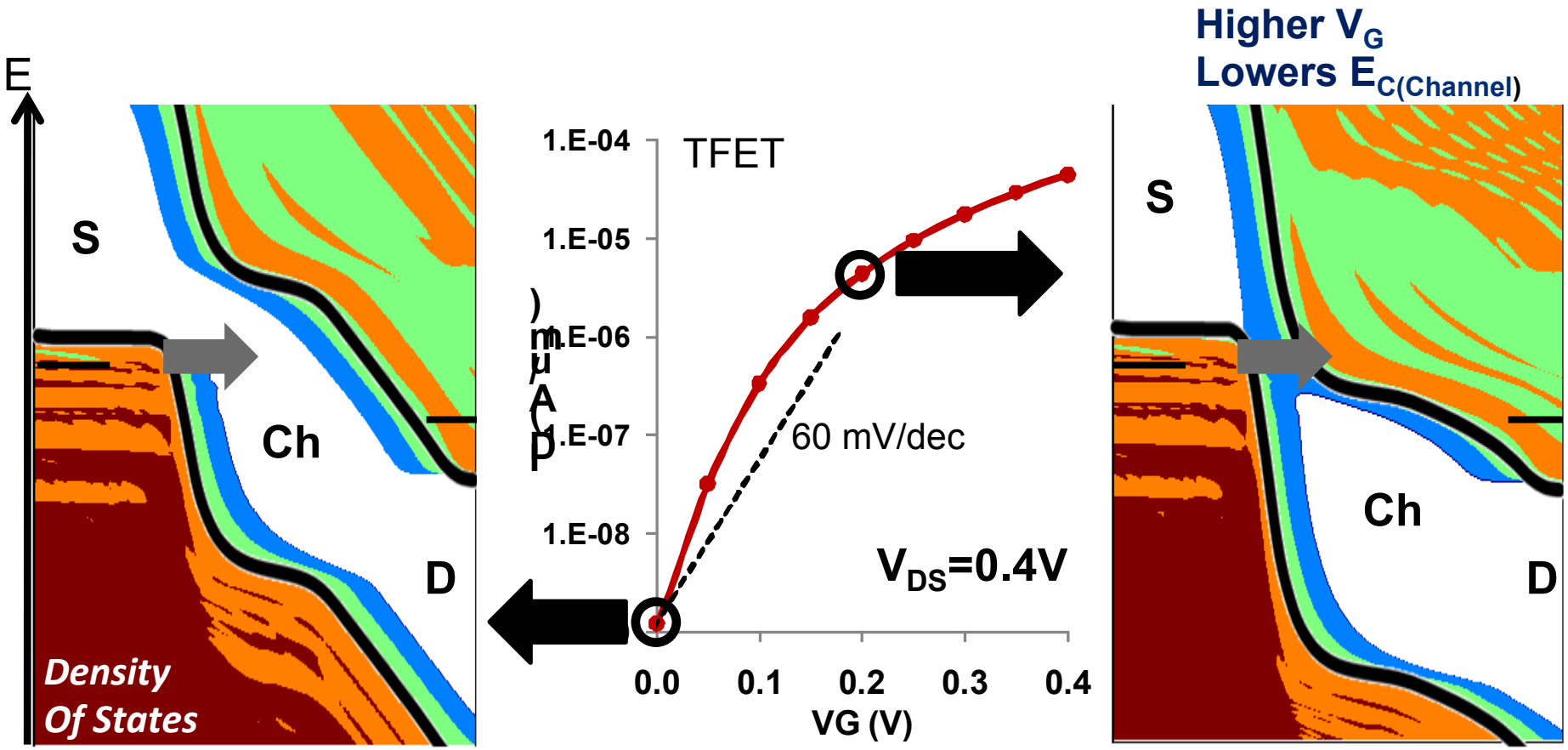
Mapping the Pathways to "Beyond–CMOS" Technology for Computation

Ian Young
Senior Fellow, Technology and Manufacturing Group,
Director, Exploratory Integrated Circuits,
Components Research
Intel Corporation
Hillsboro, Oregon


32bit adder
Energy, fJ
Delay, ps
10 3
10 2
10 1
10 0
10 -1
10 2
10 3
10 4
10 5
10 6
ASL
CSL
STOlogic
Spin torque
Ferroe lectric
MITFET
FEFET
STT/DW
NML
CMOS HP
SpinFET
GpnJ
vdWFET
ITFET
HetJTFET
NCFET
ExFET
TMDTFET
CMOS LV
PiezoFET
gnrTFET
ThinTFET
HomJTFET
SMG
SWD
Magneto electric
GaNTFET
BisFET
Tunneling
Slower, but non-volatile
CMOS ref
Electronic
Spintronic
Ferroelectric
Orbitronic
Straintronic

TFET Sub-threshold Slope

•Tunneling probability increases sharply at the onset of Source Valance Band and Channel Conduction Band overlap



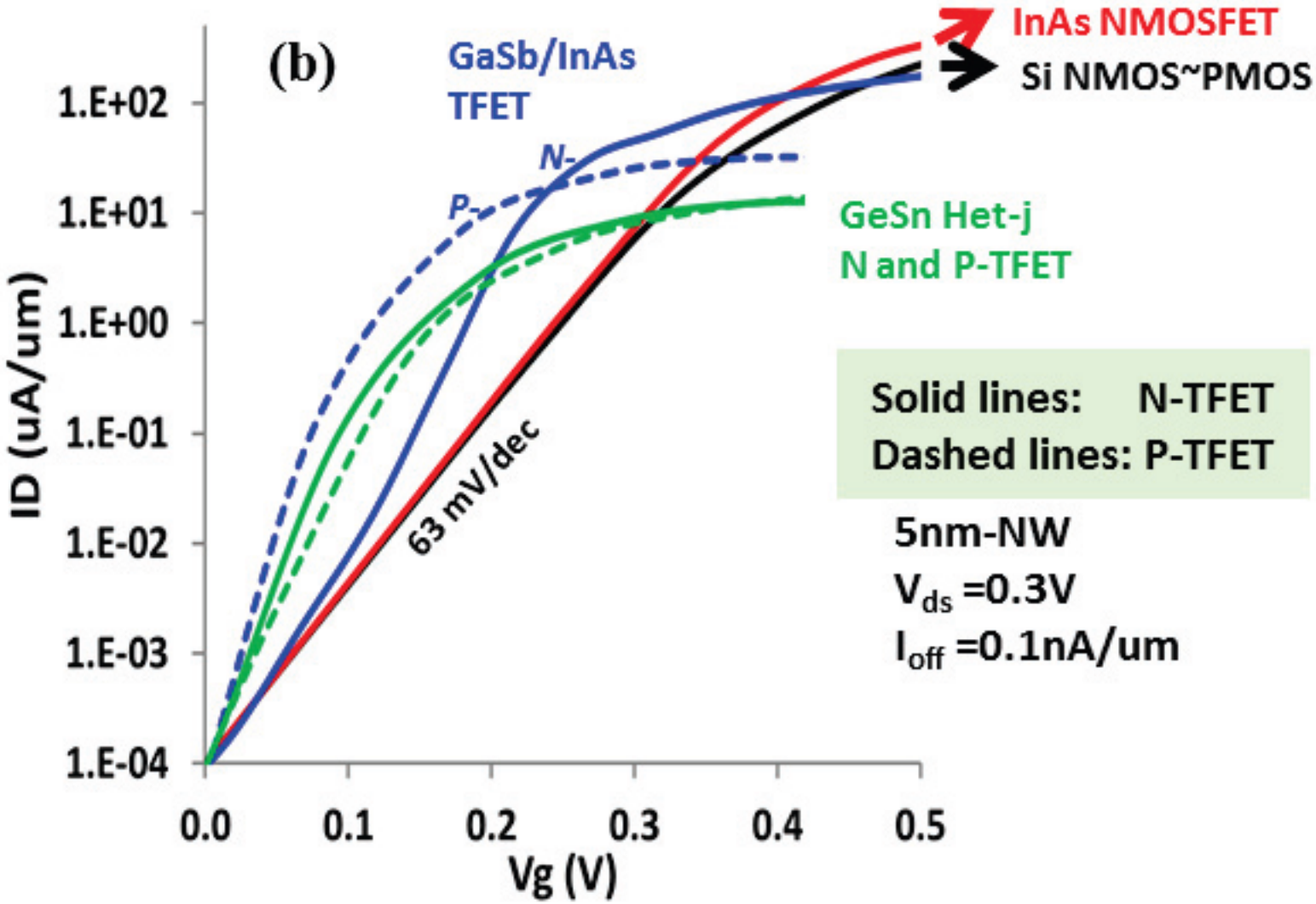
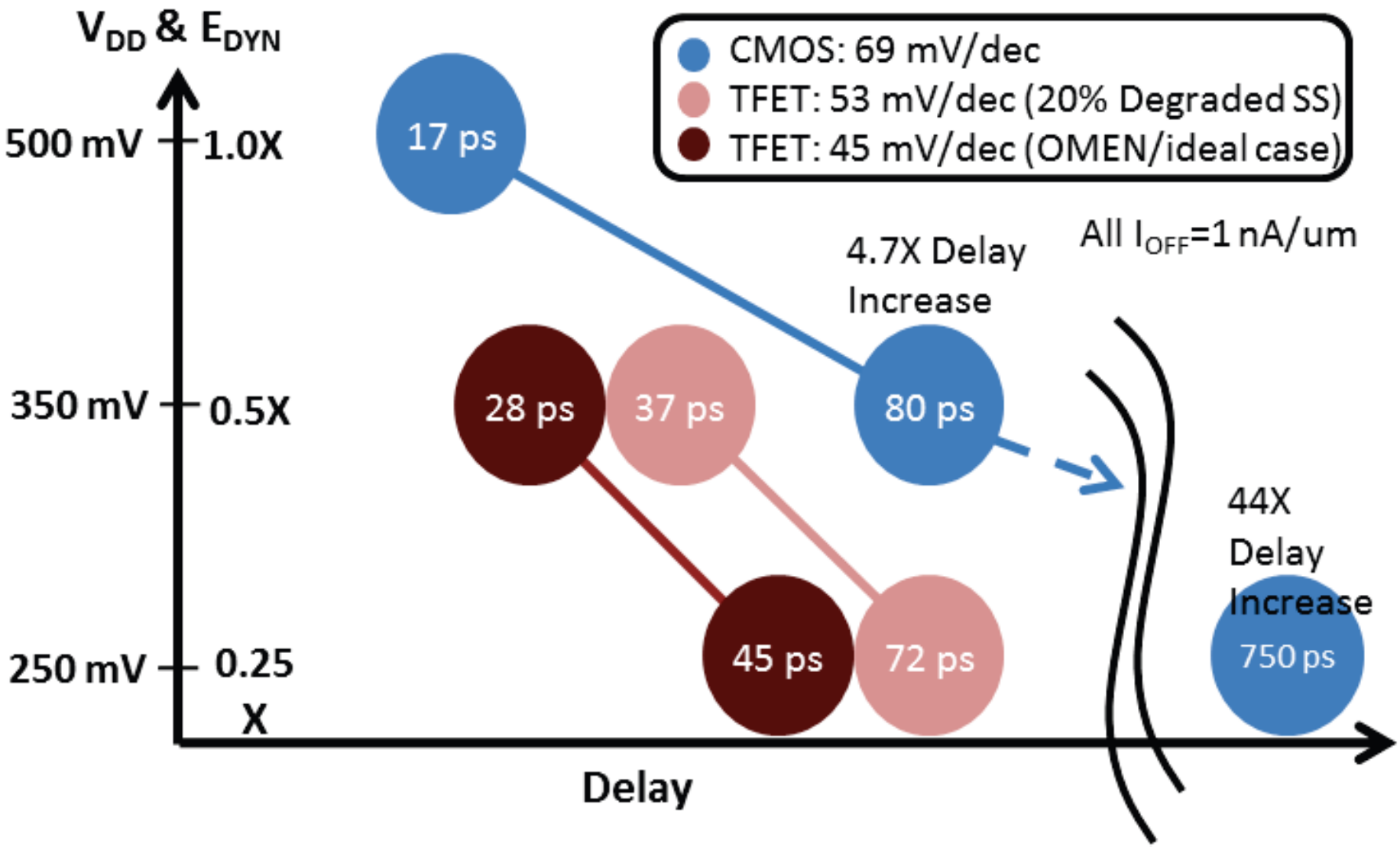
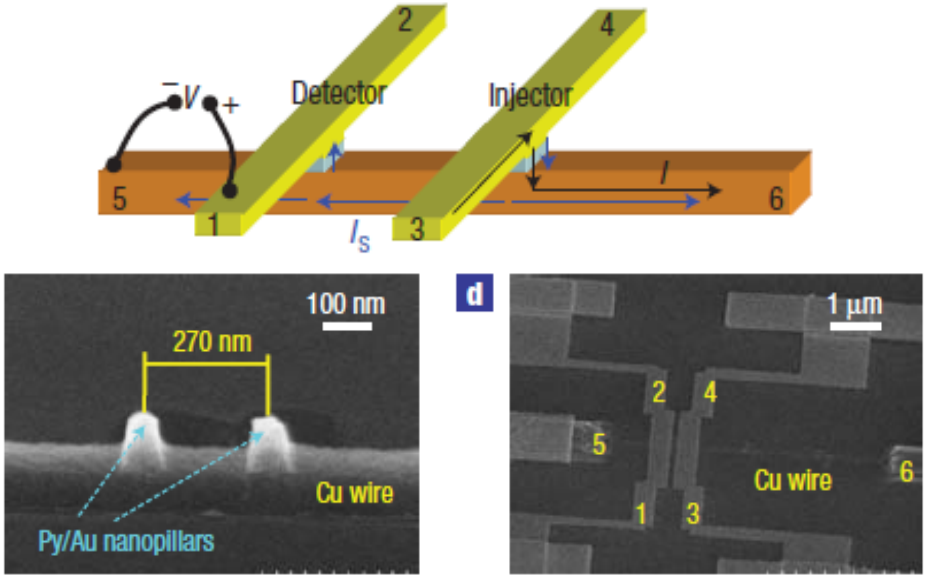


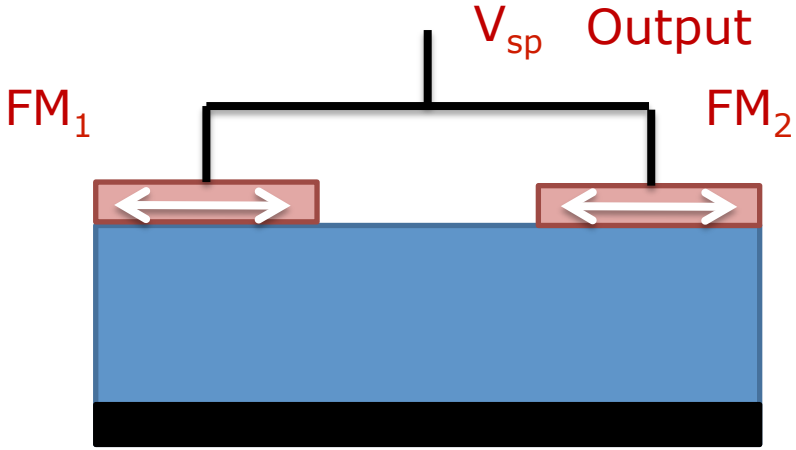
Figure 1: (a) TFET vs MOSFET structure and principle of operation: drive-current (transport) defined by tunneling, steep-SS due to filtering of high-energy carriers. (b) IDS vs VGS for GaSb/InAs het-jn. N- and P-TFET, GeSn het-jn. N- and P-TFET compared with Si and InAs MOSFET


V_{DD} & E_{DYN}
500 mV
1.0X
350 mV
0.5X
250 mV
0.25 X
Delay
CMOS: 69 mV/dec
TFET: 53 mV/dec (20% Degraded SS)
TFET: 45 mV/dec (OMEN/ideal case)
All I_{OFF}=1 nA/um
17 ps
4.7X Delay Increase
80 ps
28 ps
37 ps
45 ps
72 ps
44X Delay Increase
750 ps

Spin logic device based on spin torque

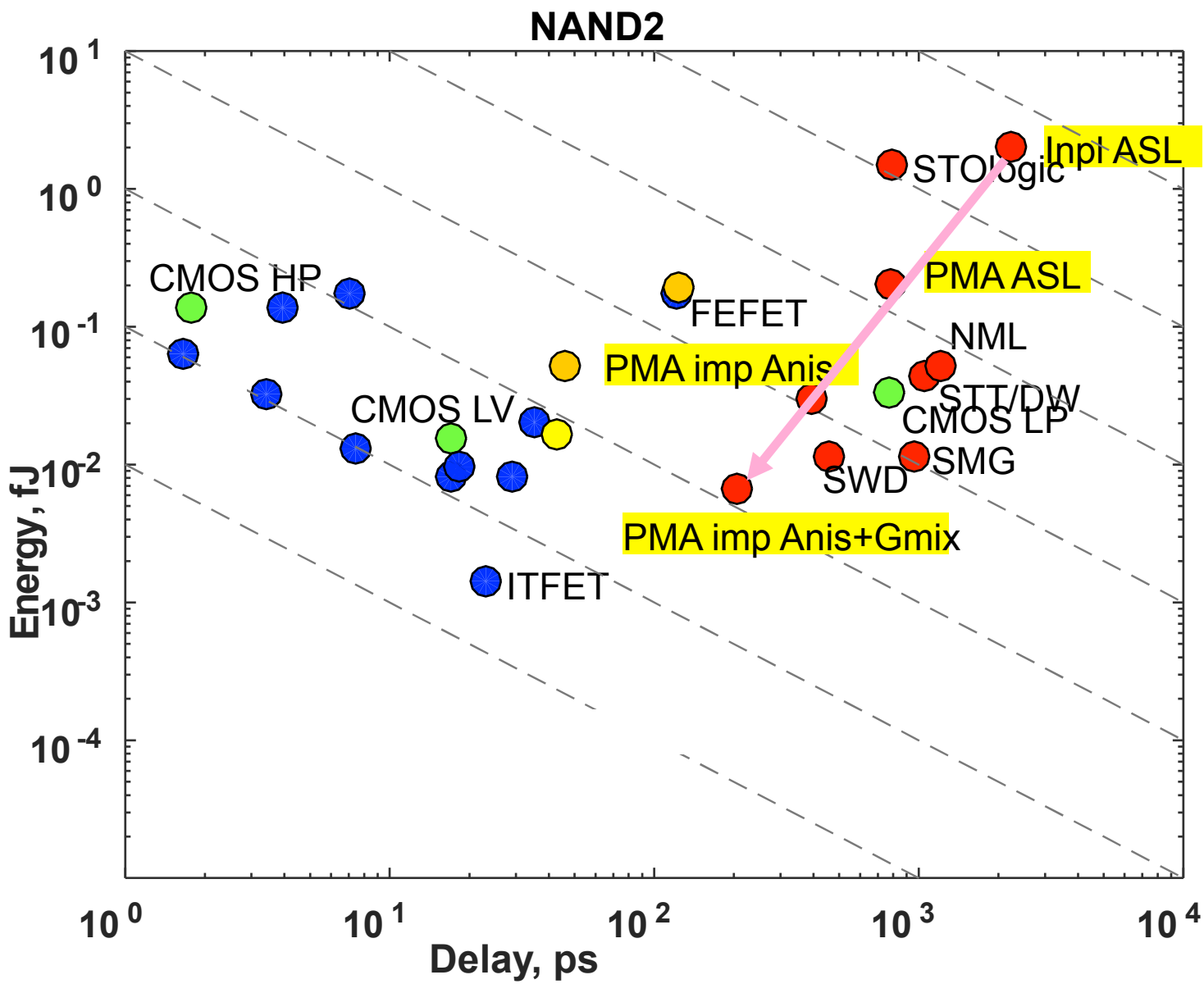


Nature Physics 4, 851 - 854 (2008)



Proposed all Spin Logic Device (ASL)

Nature Nano 5, 266 (2010).



D. E. Nikonov, I. A. Young, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits 2015

Summary:

- Benchmarking of Beyond-CMOS Devices is useful to explore new device concepts.
- Spin Logic is an interesting device due to low operating voltage and non-volatility.
  - Needs materials and circuit research
- Tunneling FET an attractive option for replacing CMOS due to it's steep sub-threshold slope and charge token like CMOS

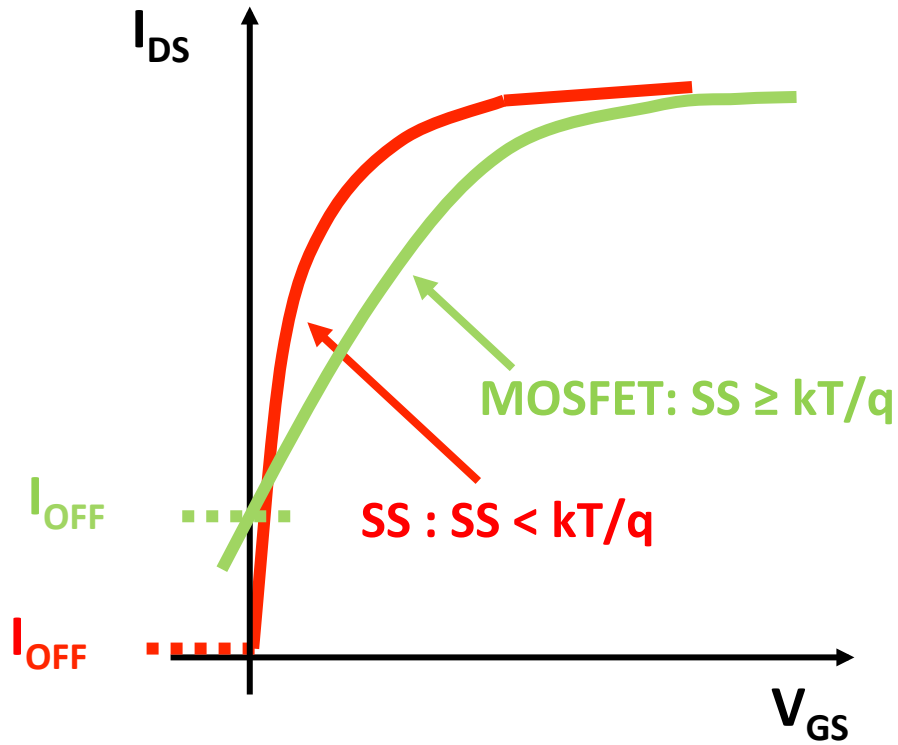
Recent Progress in Steep Slope Transistors

Suman Datta

Pennsylvania State University, University Park, PA, USA
University of Notre Dame, Notre Dame, IN, USA

PENNSTATE
1855

Steep Slope (SS) FETs



✓ **SS FETs to enable continued or accelerated supply voltage scaling**

Steep slope FETs

$$SS \approx \ln 10 \left[\frac{1}{V_{TW}} \frac{dV_{TW}}{dV_{GS}} + \frac{\xi + b}{\xi^2} \frac{d\xi}{dV_{GS}} \right] - c_V \frac{d\psi_S}{dV_{GS}} - c_Q \frac{dn_S}{dV_{GS}}$$

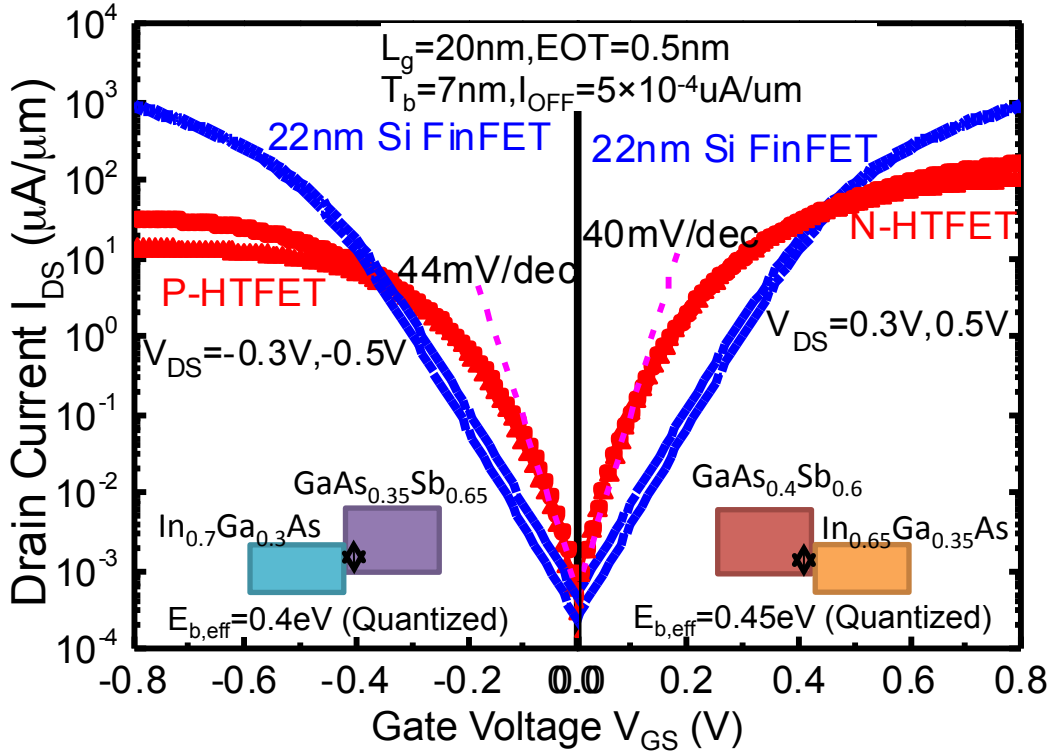
interband tunneling using energy filtering

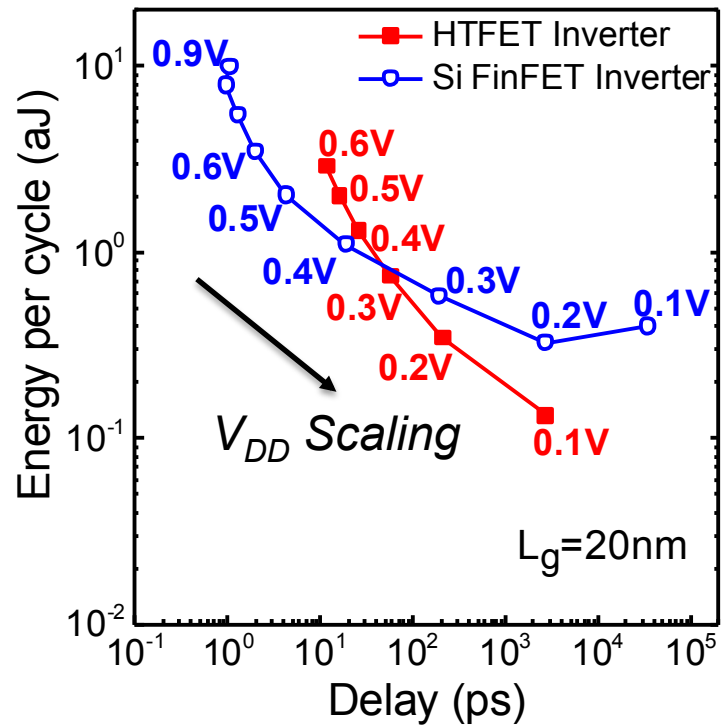
voltage-gain using negative capacitance

carrier gain using correlation, phase transition

LEAST Starnet center (SRC and DARPA) at Notre Dame focuses on demonstrating steep slope FETs

HTFET inverter: Energy Delay Promise



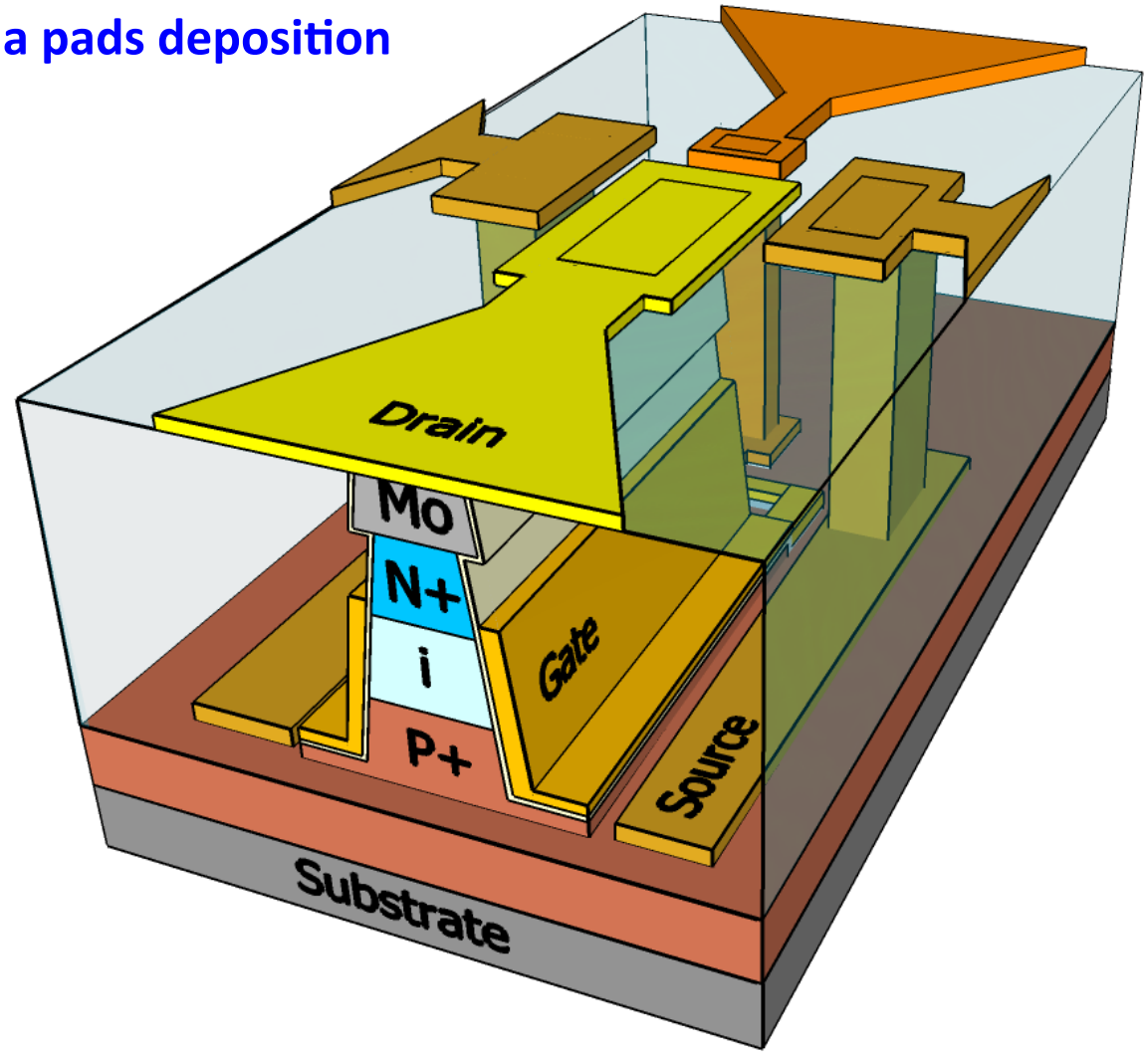


✓ **HTFET inverter shows energy efficient operation over CMOS at ultra low V_{DD} application (in theory)**

Courtesy: H. Liu

HTFET Demonstration Platform

Gate, Source via pads deposition



Take Aways

- Tunnel FETs
  - **Materials: interface defect control**
  - Devices: scaling, layout, variation
  - Circuits: leverage sub-threshold CMOS design techniques
  - Architecture: heterogenous mixed core targeting dim silicon
- Negative Capacitance FETs
  - **Materials: scaling, switching speed, history effect**
  - Devices: variation, aging, endurance
  - Circuits and Architecture: tuning hysteresis, exploiting non volatilty
- Phase Transition FETs
  - **Materials: thermal stability, on-off conductance ratio**
  - Devices: monolithic integration, switching speed
  - Circuits and Architecture: low power digital CMOS and beyond (neuromorphic, coupled oscillators)

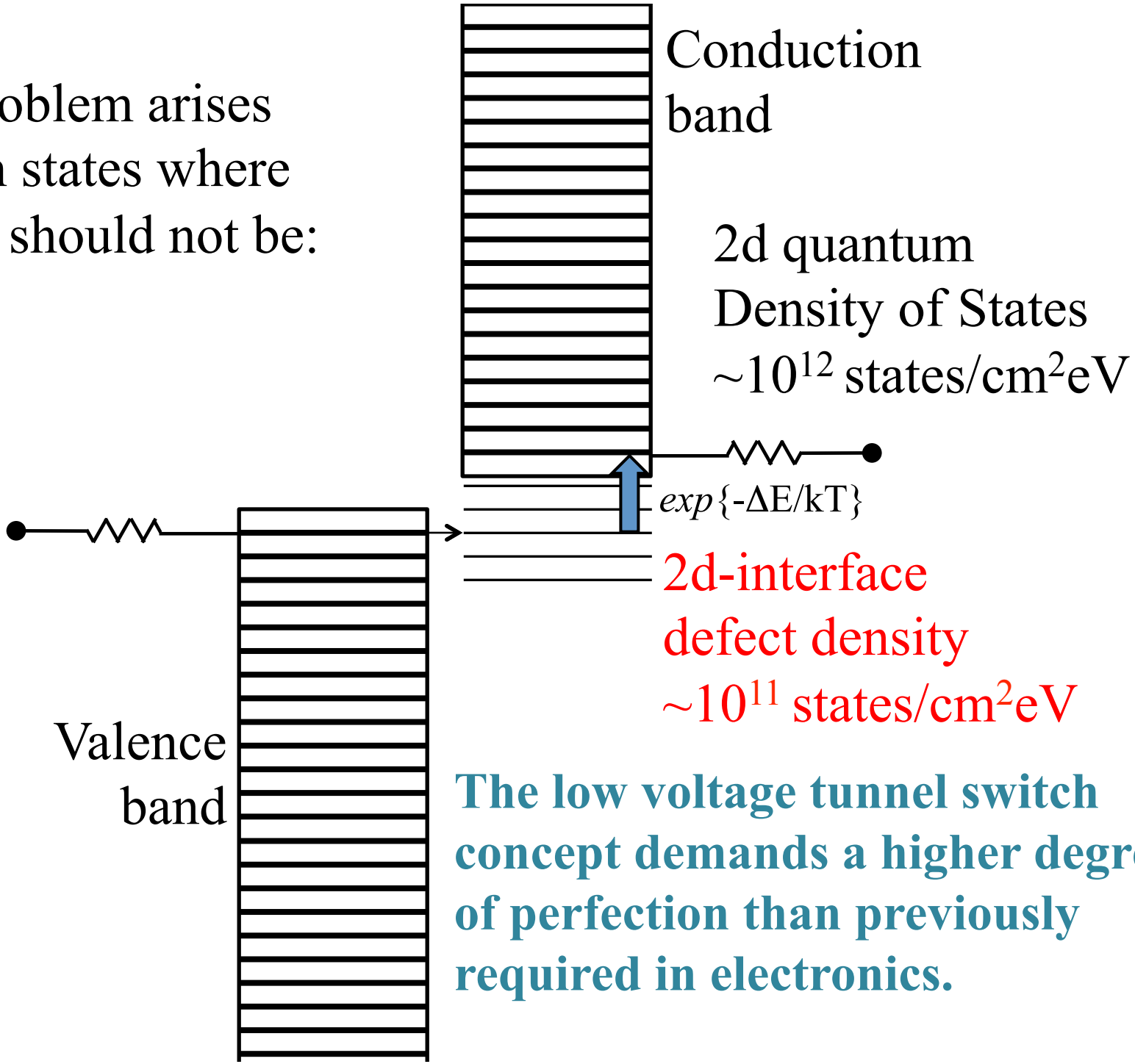
Moore's Law for Energy: Searching for a milli-Volt Switch

Eli Yablonovitch,
Director, NSF Center for
Energy Efficient Electronics Science

Rebooting Computing Summit 4
Washington DC
Dec. 11, 2015

Berkeley UNIVERSITY OF CALIFORNIA
Massachusetts Institute of Technology
STANFORD UNIVERSITY
THE UNIVERSITY OF TEXAS AT EL PASO
FLORIDA INTERNATIONAL UNIVERSITY
CALIFORNIA COMMUNITY COLLEGES CHANCELLOR'S OFFICE

A problem arises from states where they should not be:



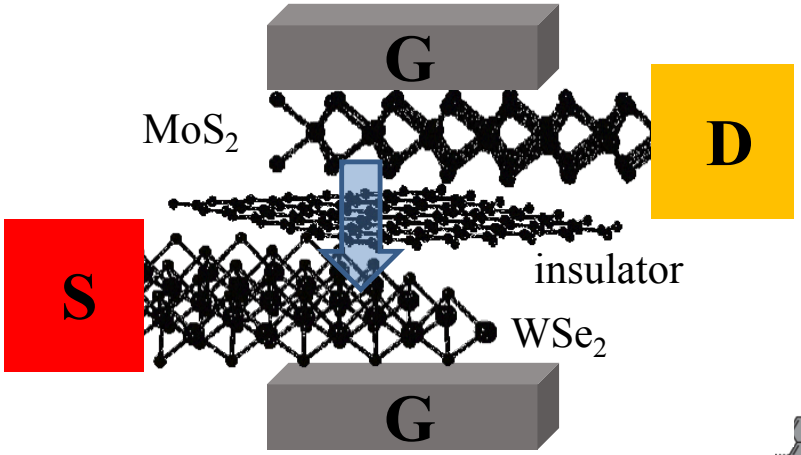
The low voltage tunnel switch concept demands a higher degree of perfection than previously required in electronics.

A much more chemical approach is needed

- We are placing attention squarely on novel materials systems capable of producing the most perfect molecular scale device structures, that will be a pre-requisite for future progress.
  - chalcogenide monolayer structures
  - molecular synthesized structures

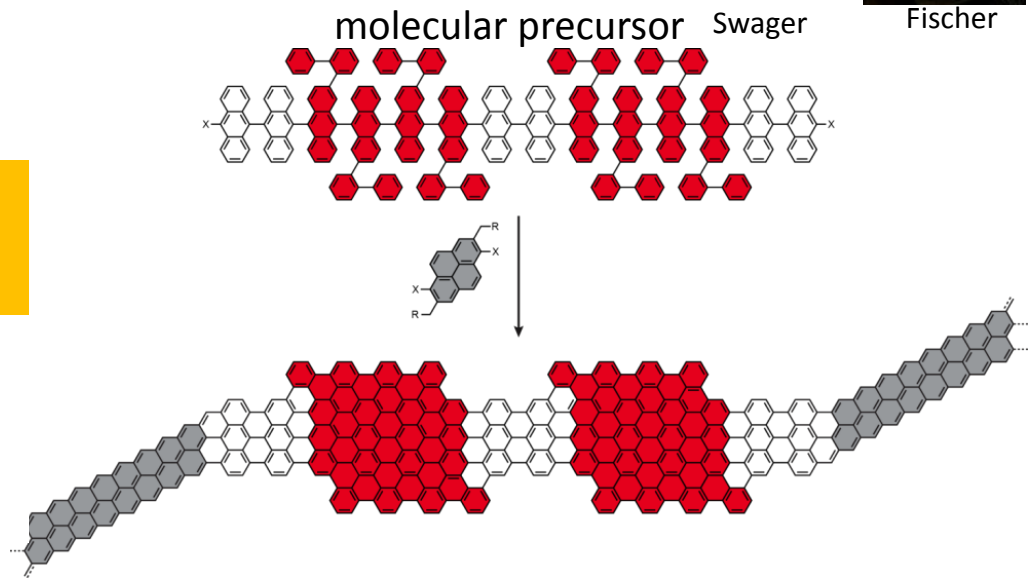
Ali Javey

Yablonovitch



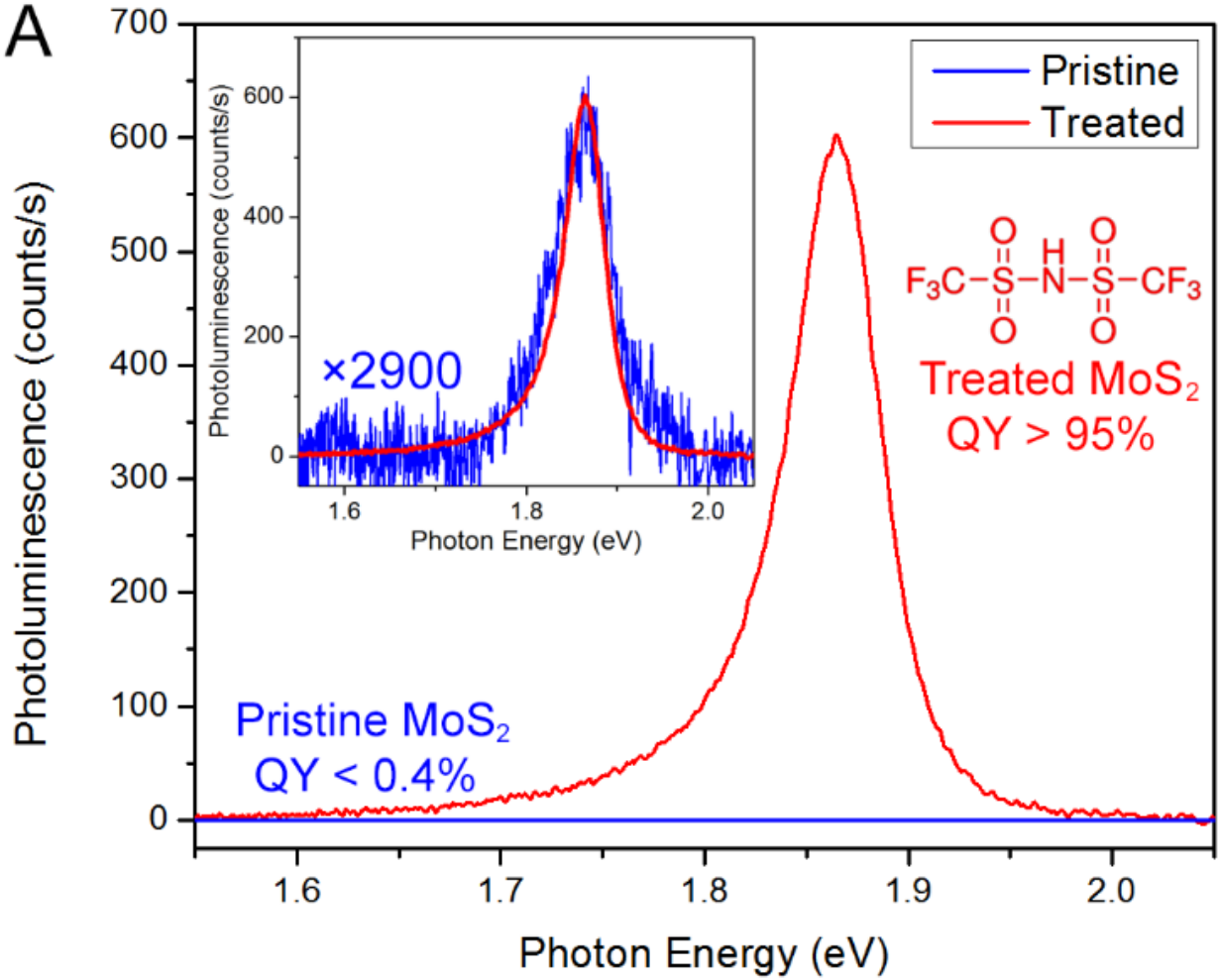
Swager

Fischer



double quantum dot graphene

By **chemical treatment** we have raised the luminescence efficiency of monolayer MoS_2 by orders of magnitude to >95%



A. Javey et al, SCIENCE 350, 1065 (Nov. 2015)

Summary

1. The Moore's Law for miniaturization will be replaced by the Moore's Law for Energy.

2. There is up to a $10^6\times$ reduction available.

3. This will require new Materials Science, including improvement in the new 2d monolayer semiconductors.

4. New architectures would be nice, but the current architecture can be preserved.

Microsystems
Science, Technology & Components

Overview of Emerging Research Memory Devices

2015 ITRS-ERD Meeting

Bridging the Research Gap between Emerging Architectures and Devices

February 26, 2015

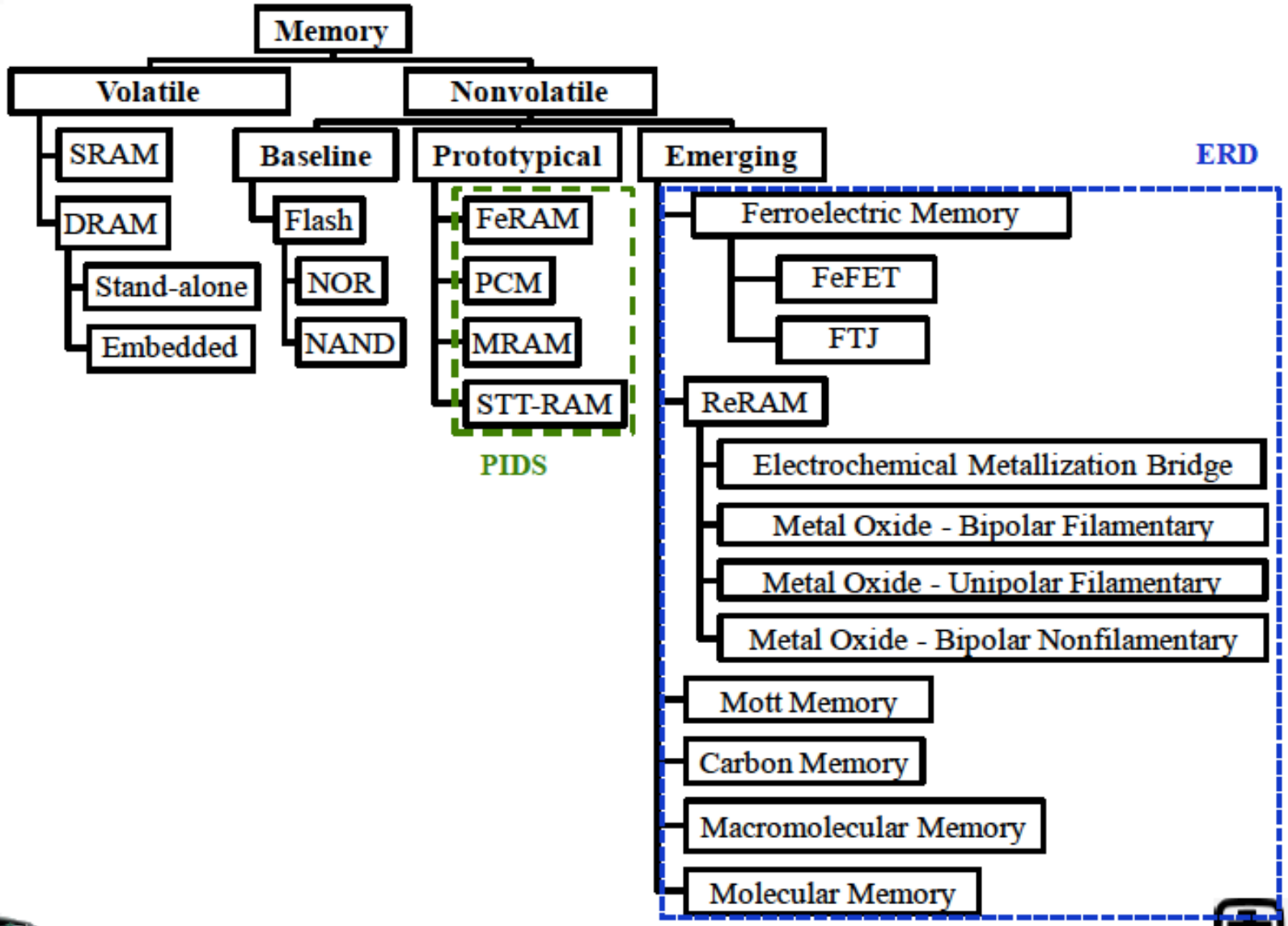
Matthew Marinella
Sandia National Laboratories
matthew.marinella@sandia.gov

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

ITRS

Sandia National Laboratories

2013 ERD Memory Entries



Key Updates to 2013

- Updated all tables with current values from the literature
- Split ReRAM into four individual categories
  - Electrochemical Metallization
  - Metal-oxide Bipolar Filamentary
  - Metal-oxide Unipolar Filamentary
  - Metal-oxide Bipolar Nonfilamentary
- Split Ferroelectric Memory into two categories
- Removed nanoelectrical-mechanical systems (NEMS) based memory due to lack of research progress
- Added carbon memory
- Added write-energy

Present 2015-2030 Roadmap

- FinFET good for 5+5 years to 2025
- 2005. NRI: New Switch
  - Technology reuse: cousins of CMOS
  - Explore magneto-electric effects
- 2010. TFET looks promising, effort increased
  - New magneto-electric devices proposed
  - Memory options on the raise
- 2015. TFET good for 2020-2025 coexistence with CMOS
  - Increase effort on magneto-electric likely winner(s)
  - 3D memory in production
  - Resistive memory very promising
- 2020. Magneto-electric earliest insertion
  - Some new memory makes it big

Needs

Research Facilities capable of full device process capability