Technology for the next 20-30 years and beyond

Greg Yeric, Arm Research

10 Nov 2017
Moore’s Law: we can get a dozen more years...for some
So everything is just fine, right?
Standard Cell scaling... 4, 3, 2 fins per transistor

> 0.7x linear shrink
+ track height reduction

plus taller fins
“scaling boosters”

Contact over active gate is a revolutionary feature for another ~10% area scaling.

TECHNOLOGY AND MANUFACTURING DAY
To continue the roadmap: High NA EUV?

High-NA optics design concepts available
Larger elements with tighter specifications, no showstoppers

Extreme aspheres enabling further improved wavefront / imaging performance
Tight surface specifications enabling low straylight / high contrast imaging
Big last mirror driven by High NA

Wafer level
NA > 0.5

Design examples
Moore’s Law: we can get a dozen more years...for some

- EUV works (or 6x MP works)
- High NA EUV works
- Gate-All-Around (GAA) FETs work, 1.4nm node ≠ 1.4, 2.4, or 3.4nm $L_G$
- A few extra tricks thrown in ... and ... viola! .. 1.4nm
- With enough volume, can overcome NRE
- Moore: OK. Dennard?
“2.5D” and 3DIC hitting the mainstream: “3D-SIC”

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected”
- Gordon Moore, 1965

Nvidia Pascal claim: >3x GBps/watt improvement.

Design and package overhead are offset by increased die per wafer and higher yield.
3D-SoC with wafer bonding

- 90nm CIS
- 30nm DRAM
- 40nm logic

19.3MP @ 1/120 second
960 fps movie mode
Roadmap to per-pixel (~1um)

Impact and Design Guideline of Monolithic 3-D IC at the 7-nm Technology Node

Kyoungwook Chang, Kartik Acharya, Sourabh Sinha, Brian Cline, Greg Yeric, and Sung Kyu Lim, Senior Member, IEEE

Abstract—Monolithic 3-D (MSD) IC is one of the potential technologies to break through the challenges of continued circuit power and performance scaling. In this paper, for the first time, we demonstrate the power benefits of MSD and present design guideline in a 7-nm FinFET technology node. The predictive 7-nm process design kit (PDK) and the standard cell library using both high-performance (HP) and low-standby-power (LSTP) device technologies are developed based on NanGate 45-nm PDK, using accurate dimensional, material, and electrical parameters from publications and a commercial-grade tool flow. We implement full-chip MSD designs utilizing industry-standard physical design tools, and gauge the impact of MSD technology on performance, power, and area metrics. We also provide the design guidelines as well as a new partitioning methodology to improve MSD design quality. This paper shows that MSD designs outperform 2-D counterparts by 16% and 16.5% on average in terms of isoperformance total power reduction with 7-nm HP and LSTP cell library, respectively. This demonstrates the power benefits of MSD technology in both HP and low-power future generation devices.

Fig. 1. Structure of MSD IC based on FinFET transistors.
Increasing confinement in CMOS

- Enhanced mobility channel materials may improve things by 10-20%
- 5nm and 3nm will be extremely challenged to increase performance
3D stacking at the transistor level

1 Moore’s Law node
(just don’t think about the wiring)

CMOS Inverter: 5/3nm

Image courtesy: imec
3D stacking at the transistor level

Complex stacked CMOS

Images courtesy: imec
3D-SiC to 3D-SoC:

3D-IC design disrupts a large set of existing practices:

• Partitioning across 3D tiers will include signals, redistribution and power meshes, and shielding.
• This will require 3D-enablement in STA, schematic capture, PnR, DRC/LVS, PEX, and IR/EM checks, DFT / DFR, thermal and stress analysis, functional verification, assembly, yield and supply chain management.
eNVM contenders: No “supermemory” ... yet

- **PCM:**
  - Variability
  - Endurance

- **MRAM:**
  - Power/speed
  - Disturb
  - Cost

- **Filamentary RRAM:**
  - Variability
  - Endurance
  - Scalability

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**Filamentary RRAM**:

- Variability
- Endurance
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Out of fab

Form (4V)

Set (-2V)

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S. Ikeda, et al., IEDM 2014

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IBM
Putting it together: 3D-SoC with “e”NVM

Three-dimensional integration of nanotechnologies for computing and data storage on a single chip

Max M. Shulaker$^1$,$^2$, Gage Hills$^1$, Rebecca S. Park$^1$, Roger T. Howe$^1$, Krishna Saraswat$^1$, H.-S. Philip Wong$^1$ & Subhasish Mitra$^{1,3}$

Courtesy: Stanford
Putting it together: 3D-SoC with “e”NVM

1M sensors
1Mb RRAM
2M CNT-FETs

Toward 1000x EDP, especially for data-rich applications where >85% of the clock cycles are for memory

“interwoven compute + memory + sensing”

Increasing diversity of computing, built on 2D CMOS, enabled by 3DIC

Courtesy: Stanford
DARPA’s Electronics Resurgence Initiative

“Page 3 investments”

3DIC + NVM intra-layer capabilities:
9M interconnects/mm², 50Tb/s, 2pJ/bit.

Demonstrator goals:
➢ 50X performance at power compared with 7nm 2D CMOS
➢ 4GB NVM and 50M logic gates 200mm²
➢ Cost comparable to equivalent 2D CMOS

“I thought this guy was going to talk about 20-30 years out?”
DARPA’s Electronics Resurgence Initiative

“Page 3 investments”

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Representative “new material” timeline:

1984 GMR Effect discovered
1996 Spin Torque Transfer is proposed
1996 Motorola begins MRAM research
1998 First Motorola MTJ
1999 Motorola develops 256Kb MRAM Test Chip
2002 Toggle patent granted to Motorola
2004 Motorola separates semiconductor business into Freescale Semiconductor
2006 Industry first MRAM (4Mb) product commercially available
2008 Freescale spins out MRAM business as Everspin Technologies
2010 Everspin qualifies industry first embedded MRAM
2010 Everspin releases 16Mb density
2012 Everspin produces 64Mb ST-MRAM on a 90nm process
2016 Everspin announces 256Mb ST-MRAM to customers
2017 eMRAM samples from foundries
2018 eMRAM product for use

~30 years discovery to product
Future technology pipeline

Needs:
- Extend conventional CMOS scaling
- Accelerate device and materials R&D from suppliers, consortia, and universities
  - Proper benchmarking, relevant demonstrators
  - Manage unprecedented diversity and change

Researchers: Reboot Computing
Piezoresponse force microscopy image of the ferroelectric domain structure of \textit{multiferroic ErMnO}_3. The dark and light regions correspond to opposite orientations of the electric dipoles. The vertical dimension is about 20 \textmu m.

Image courtesy of Manfred Fiebig and Martin Lilienblum (ETH Zürich)

Fundamental Materials Research and the Course of Human Civilization

Nicola Spaldin*

\textit{Unless we change direction, we are likely to wind up where we are headed.}

(Ancient Chinese proverb)
How Materials Science Will Determine the Future of Human Civilization

by Emerging Technology from the arXiv  August 16, 2017

Why Moore’s law is set to destroy the planet and how to stop it

September 19, 2017

FUTURIST
Materials innovation: 2D (graphene)

2004: + = 2010 Nobel Prize

Andre Geim
Konstantin Novoselov
Materials revolution snapshot:  2D

Scientists Have Turned Cooking Oil Into a Material 200 Times Stronger Than Steel
Materials revolution snapshot: 2D

200 molybdenum disulfide transistors (MoS₂ FETs)
Materials revolution snapshot: 2D

*Journal of Materials Science: Materials in Electronics*

High-performance transparent ultraviolet photodetector based on thermally reduced graphene oxide and ZnO thin films

Authors: A. M. Bazargan, F. Sharif, S. Mazinani, N. Naderi
Researchers discover a magnetic 2D material

Researchers from the Lawrence Berkeley National Laboratory discovered the world’s first magnetic 2D material - chromium germanium telluride (CGT). It was debatable whether magnetism could survive in such thin materials - and this discovery could pave the way to extremely thin spintronics devices.
Materials revolution snapshot: 2D

Spintronics in novel 2D materials: A solution for future electronics through magnetic devices
Materials revolution snapshot: 2D

"Valleytronics' advancement could help extend Moore's Law"

By Grove Potter, phys.org
May 1st, 2017
Materials revolution snapshot: 2D

2D Materials Go Ferromagnetic, Creating a New Scientific Field

By Dexter Johnson, spectrum.ieee.org

Photo: Marilyn Chung/Berkeley Lab
Materials revolution snapshot: 2D
Materials revolution snapshot: 2D

2D Material Successfully Conducted Electricity At Nearly The Speed Of Light: Paves Future Of Quantum Computers

The experimental realization of ultrathin graphene has ushered in a new age in materials research. What started with graphene has now evolved to encompass numerous related single-atom-thick materials, which have unusual properties due to their ultra-thinness. Among these materials are transition metal dichalcogenides (TMDCs), which offer several key features not available in graphene and are emerging as next-generation semiconductors.

Now, new research shows that TMDCs could even realize topological superconductivity and thus provide a platform for quantum computing - the ultimate goal of a research group at Cornell University led by Eun-Ah Kim, associate professor of physics.

Scientists Have Turned Cooking Oil Into a Material 200 Times Stronger Than Steel

This is a schematic of an intercoated paired state, one of two topological superconducting states proposed in the latest work from the lab of Eun-Ah Kim, associate professor of physics at Cornell University. The material used is a monolayer transition metal dichalcogenide, image: Eun-Ah Kim, Cornell University.

Topological superconductivity in 2D materials could boost quantum computing

29 April 2017

You might also like...

Electrons protected from scattering in topological insulators

28 May 2013
Materials revolution snapshot: 2D
Materials revolution snapshot: 2D

Graphene coating that changes color when deformed or cracked

April 10, 2017 by Bob Yirka

PHYS.ORG
Materials revolution snapshot: 2D

Rice U researchers pave the way towards using graphene to repair spinal cord injuries

Researchers from Rice University, led by the renowned Prof. James M. Tour, are attempting to repair spinal cord injuries with the help of TexasPEG, a water soluble graphene nanoribbon dispersion. In rodents, the method has been able to restore a completely paralyzed rat to a motility score of 19 out of 21, where 21 is a perfect score. If successful in humans as well, it may be applicable to new injuries, and potentially old injuries up to 30 years in the past - restoring function and sensation in both paraplegics and quadriplegics.
Materials revolution snapshot: 2D
Materials revolution snapshot: 2D

Good vibrations no longer needed for speakers as research encourages graphene to talk

phys.org
May 4th, 2017

New research allows sound frequencies to be mixed together, amplified and equalized -- all within the same millimeter-sized device. Credit: David Horsell / University of Exeter
Materials revolution snapshot: 2D
Materials revolution snapshot: 2D
All of these 2D materials news items came in a 3-4 week span
Future technology pipeline

Needs:
- Extend conventional CMOS scaling
- Accelerate device and materials R&D from suppliers, consortia and universities
  - Proper benchmarking, relevant demonstrators
  - Manage unprecedented diversity and change

Figure of Merit

- 1971
- 2010
- 2015
- 2020
- 2025

Researchers: Reboot Computing

Foundries
Extend Moore’s Law
Summary: system scaling opportunity is out there

The (easy) path of pitch scaling is waning

New knobs are coming to the masses:
3D-SiC → 3D-SoC → 3D-IC and novel memories

New materials will enable an explosion of computing options, from efficient memory and I/O, to low cost IoT enablers.

Industry challenge:
Stem the slowing of “Moore’s Law” just long enough, while also accelerating novel devices enabled by entirely new materials, and manage all of this diversity and change.
Thank You
A word of caution on cost prediction math

7nm steppers are 50% faster than 28nm steppers

> 250 wafers per hour = < 15 seconds per wafer

Chuck moves > 1m/second (develops >10G)

3 nm X and Y accuracy*

*drop England onto the globe, align it to a precision of one brick, 5 times per second

are your circuits worthy?

Continuous improvement from all suppliers: resist, light source, mask, etch....
Moore has a better story than Dennard

Today:
we want to scale $L_G$ in order to open up more contact area
Pressure on R&D costs

Industry has its hands full with ≤ 5nm development.

The complexities of solutions for 3/2 nm solutions will be unprecedented.

Will there be any $ left for research?
FinFET → GAA Nanosheet

Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET

N. Loubet¹, T. Hook¹, P. Montanini¹, C.-W. Yeung¹, S. Kanakasabapathy¹, M. Guillom¹, T. Yamashita¹, J. Zhang¹, X. Miao¹, J. Wang¹, A. Young¹, R. Chao¹, M. Kang², Z. Liu³, S. Fan¹, B. Hamieh¹, S. Sieg¹, Y. Mignot¹, W. Xu¹, S.-C. Seo³, J. Yoo², S. Mochizuki¹, M. Sankaranapandian¹, O. Kwon¹, A. Carr¹, A. Greene¹, Y. Park², J. Frougier¹, R. Galatage³, R. Bao¹, J. Shearer¹, R. Conti¹, H. Song², D. Lee², D. Kong¹, Y. Xu¹, A. Arceo¹, Z. Bi³, P. Xu¹, R. Muthuini¹, J. Li¹, R. Wong¹, D. Brown², P. Oldiges¹, R. Robison¹, J. Arnold¹, N. Felix¹, S. Skordas¹, J. Gaudiello¹, T. Standael¹, H. Jagannathan¹, D. Corliss³, M.-H. Na¹, A. Knorr³, T. Wu¹, D. Gupta¹, S. Lian², R. Divakaruni¹, T. Gow¹, C. Labelle², S. Lee², V. Paruchuri¹, H. Bu¹, and M. Khare¹

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https://semiengineering.com/whats-after-finfets/
2D Material landscape

- Graphene