IEEE Industry Summit
on the Future of Computing

Technology for the next 20-30 years and beyond

Greg Yeric, Arm Research

10 Nov 2017

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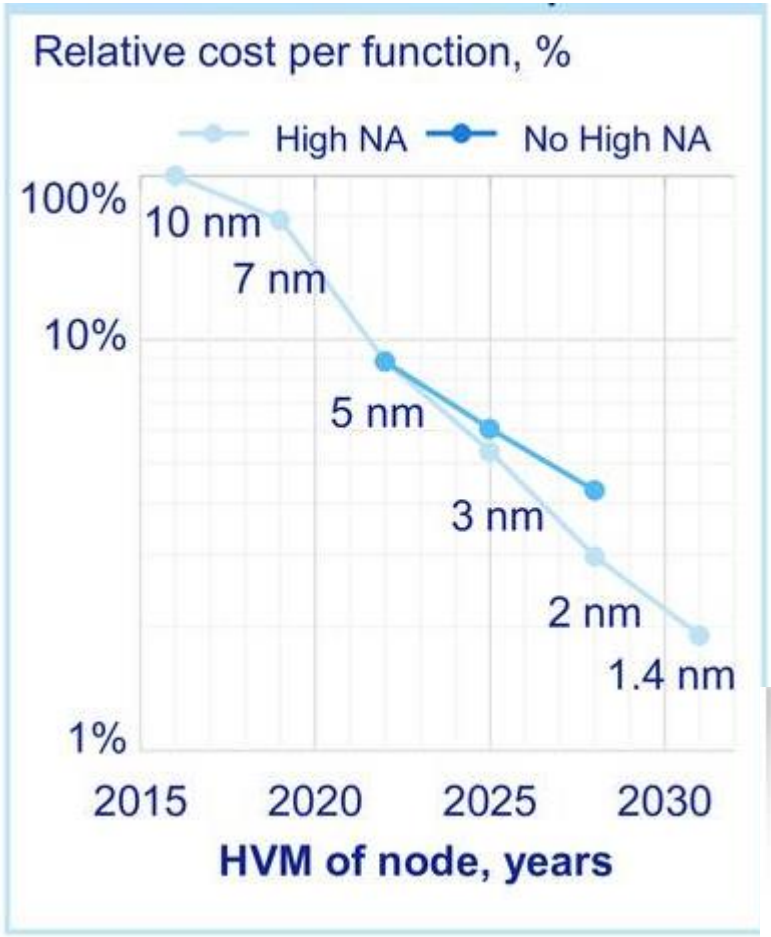
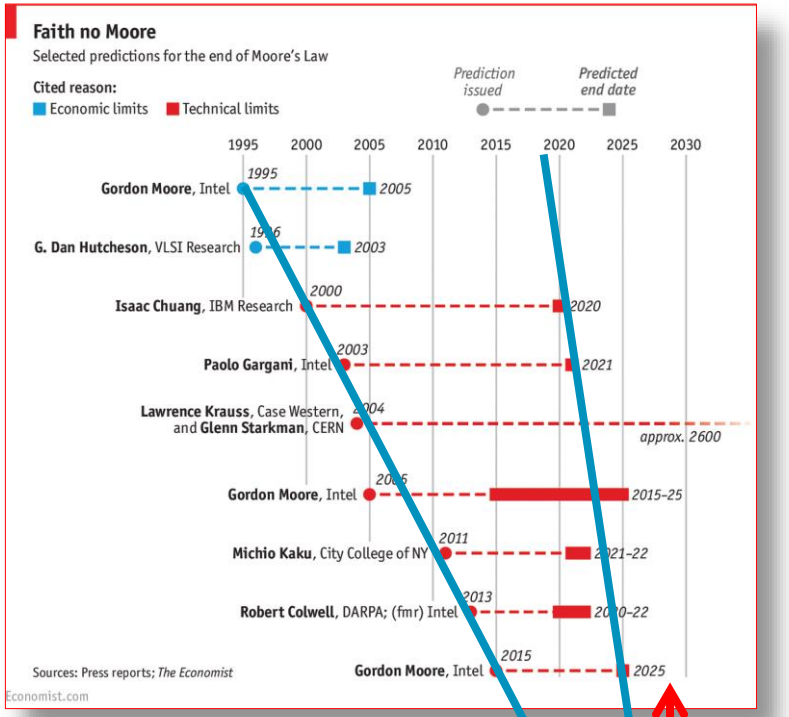
Moore's Law: we can get a dozen more years…for some



ASML

Public
Slide 35
October 31, 2016



Greg Yeric, Arm, IEDM 2015

Moore's Law ends: 2029

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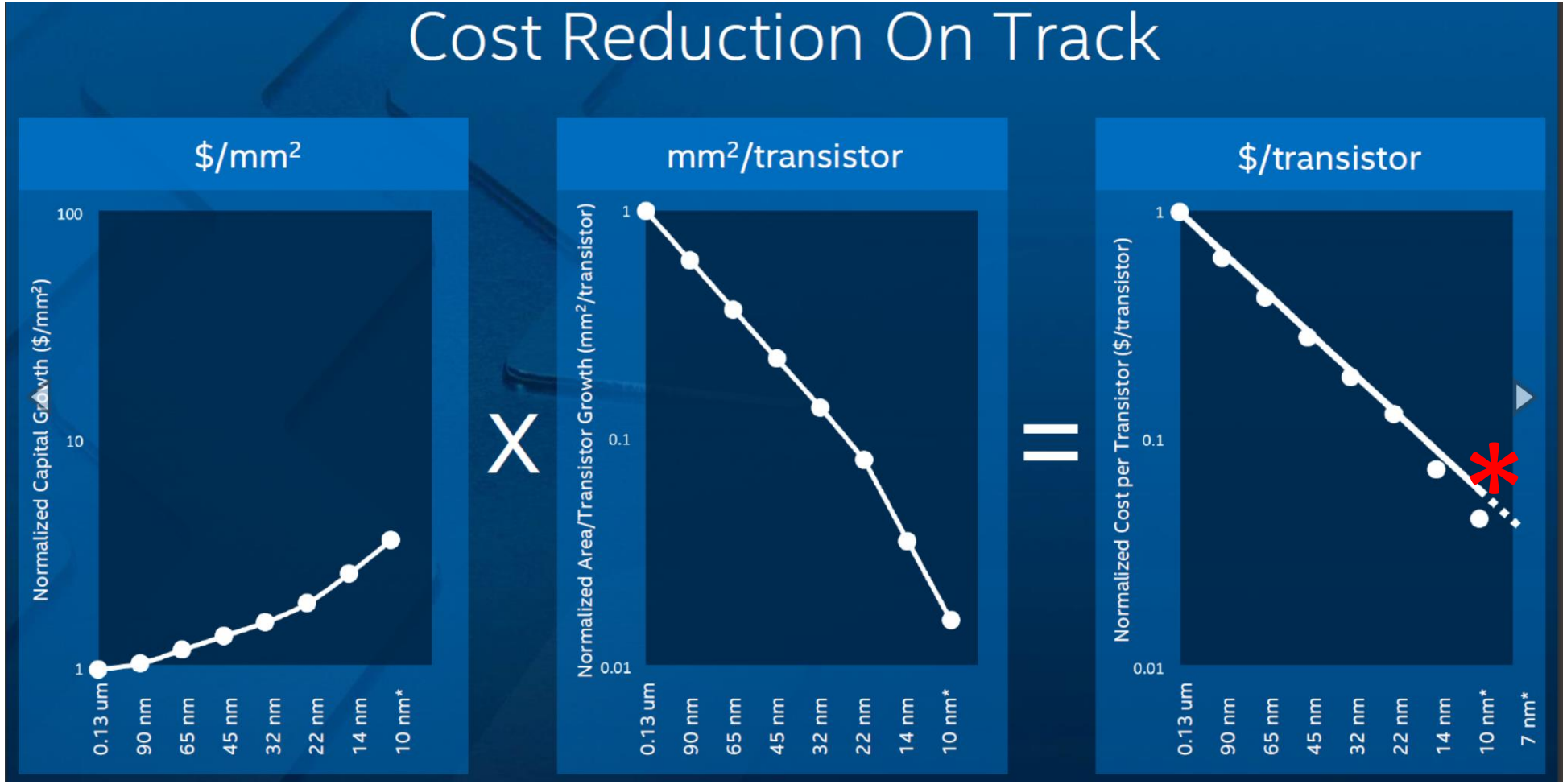
So everything is just fine, right?



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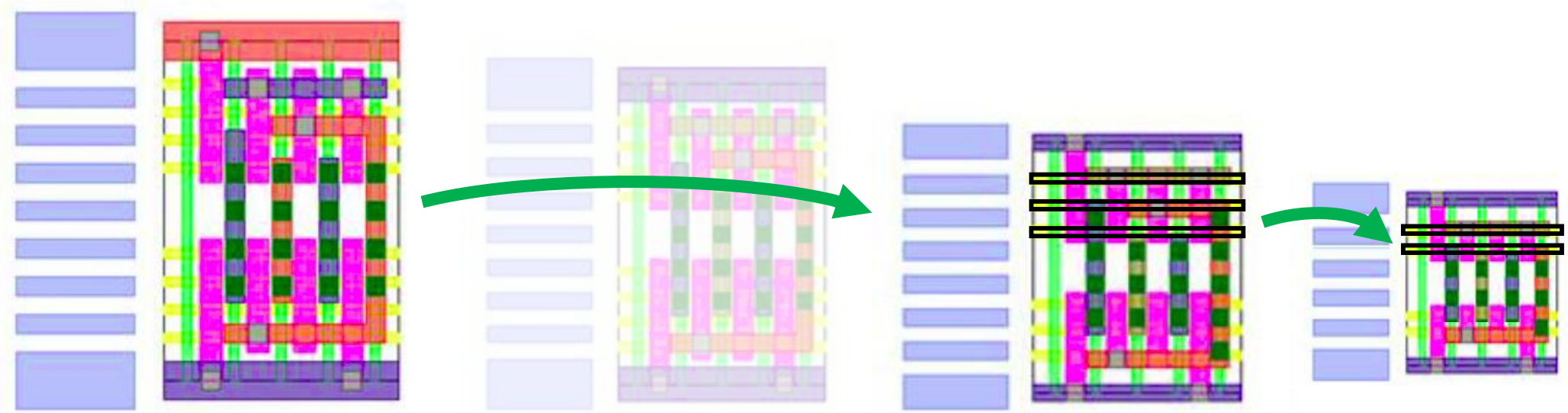
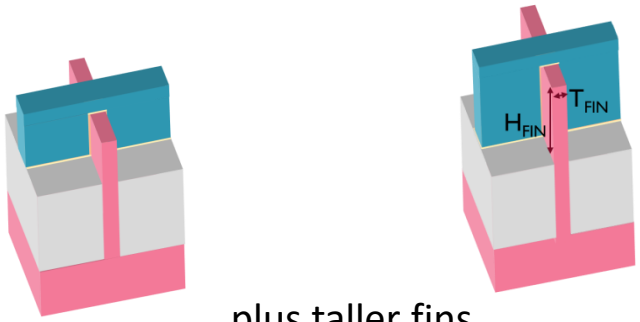
Standard Cell scaling… 4, 3, 2 fins per transistor





> 0.7x linear shrink

\+ track height reduction

plus taller fins

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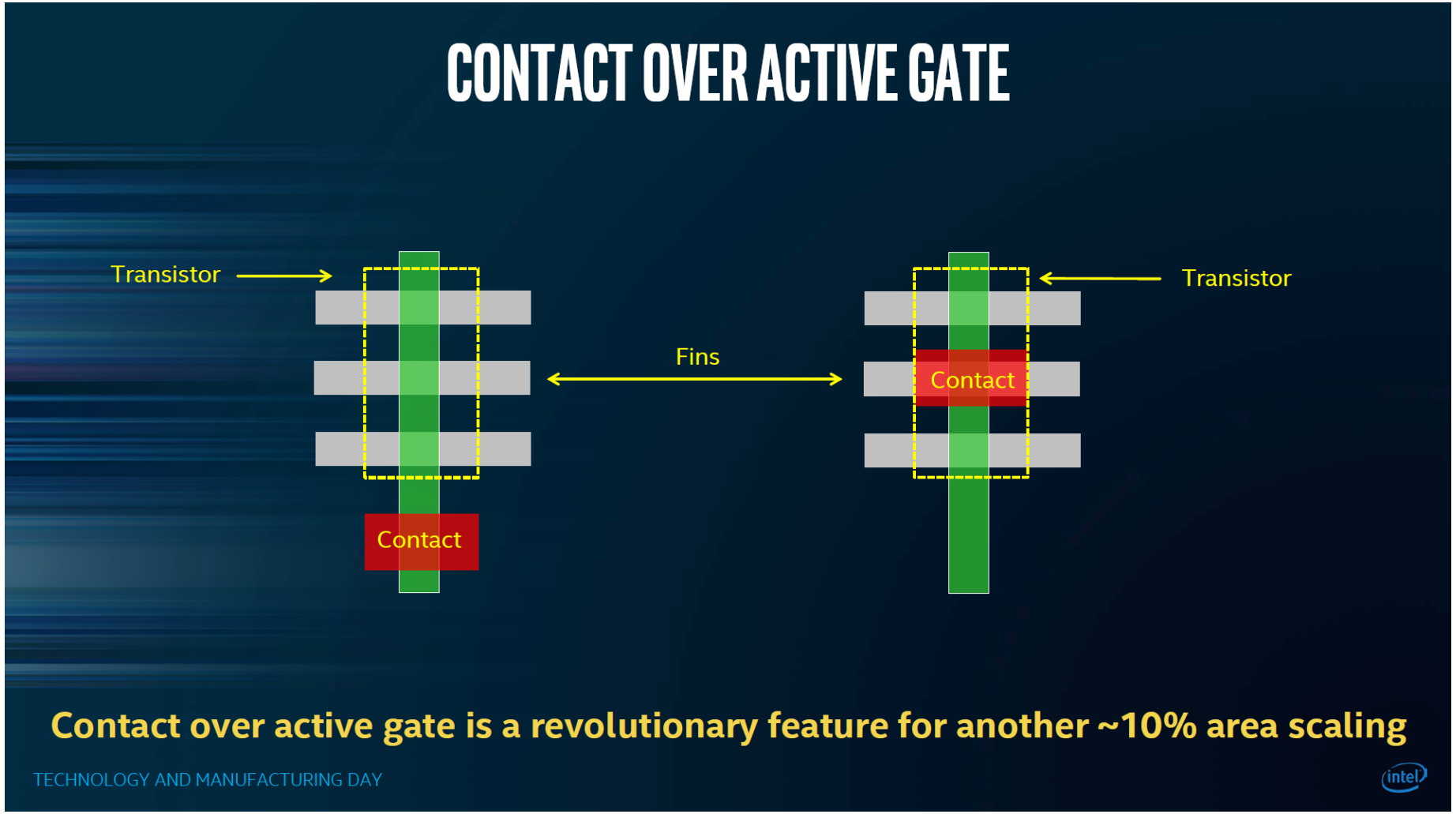
“scaling boosters”



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To continue the roadmap: High NA EUV?

High-NA optics design concepts available

Larger elements with tighter specifications, no showstoppers

ZEISS ASML

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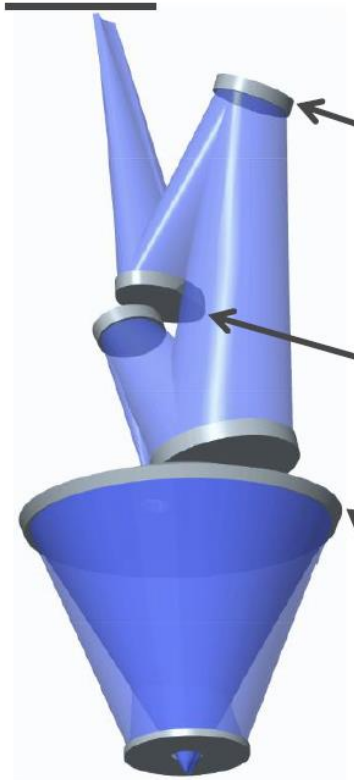
Slide 16
25 February 2016



Extreme aspheres enabling
further improved wavefront / imaging performance

Tight surface specifications enabling
low straylight / high contrast imaging

Big last mirror driven by
High NA

Wafer
leve

NA >0.5 *Design examples*

*B. Kneer, et al, "EUV lithography optics for sub-9nm resolution," Proc. SPIE **9422**, (2015).*

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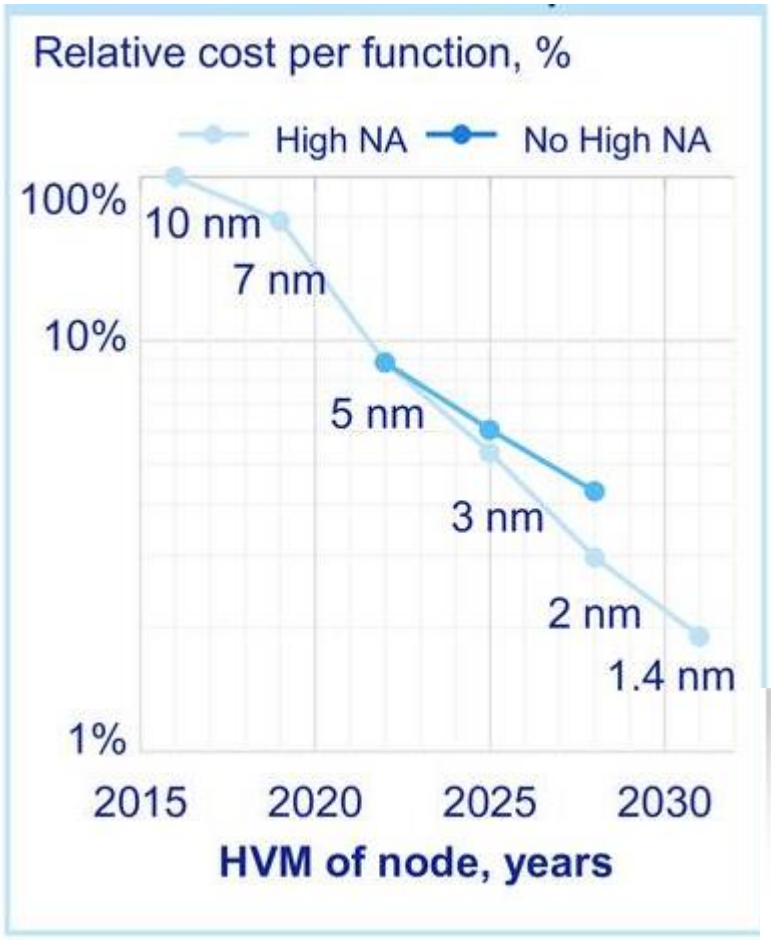
Moore's Law: we can get a dozen more years…for some



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- EUV works (or 6x MP works)
- High NA EUV works
- Gate-All-Around (GAA) FETs work, 1.4nm node ≠ 1.4, 2.4, or 3.4nm L_G
- A few extra tricks thrown in … and … viola! .. 1.4nm
- With enough volume, can overcome NRE
- Moore: OK. Dennard?

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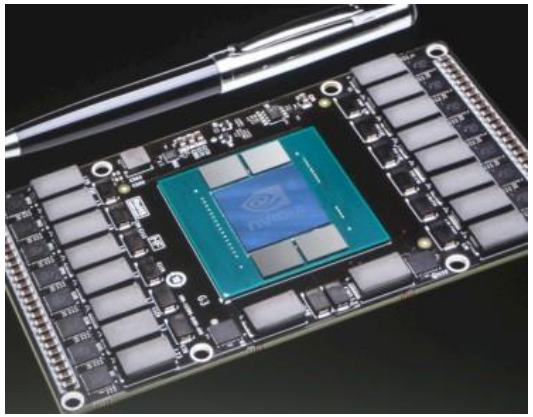
Pitch Scaling
New
eNVM
3DIC

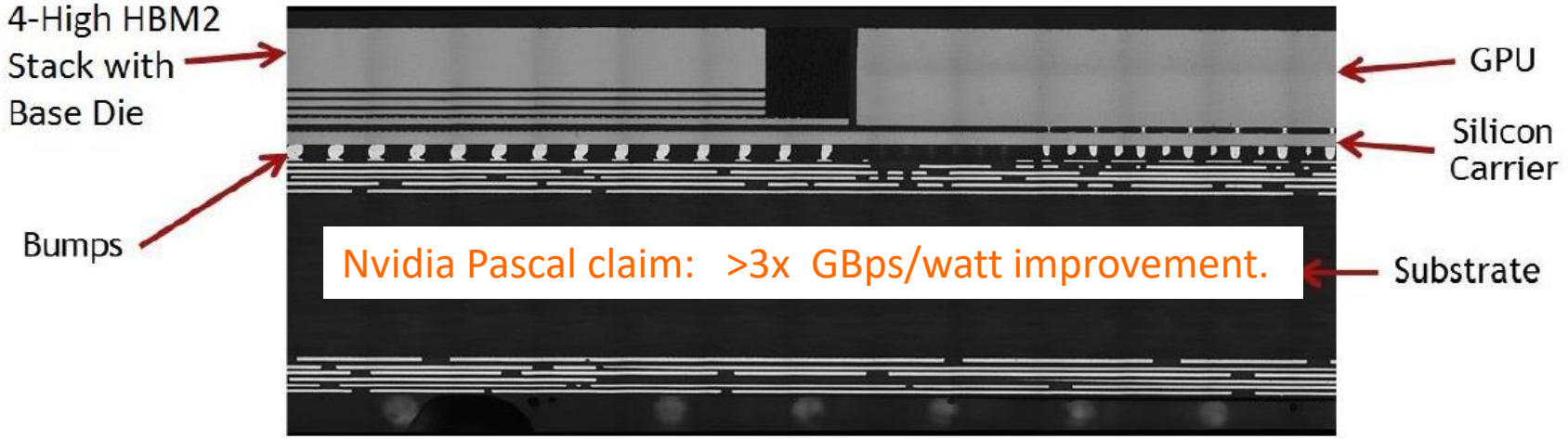
“2.5D” and 3DIC hitting the mainstream: “3D-SIC”

	3D-SIC		
3D-Wiring level	Global	Sem	
Partitioning	Die	bloc	
3D Technology	Die stacking Die-to-Wafer stacks Die-to-Si-interposer	Para	Wafer-to-Wafer bonding	Active layer bonding or deposition

E. Beyne, IEEE Design & Test, May/June 2016

> “It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected”
>
> - Gordon Moore, 1965





Design and package overhead are offset by increased die per wafer and higher yield.

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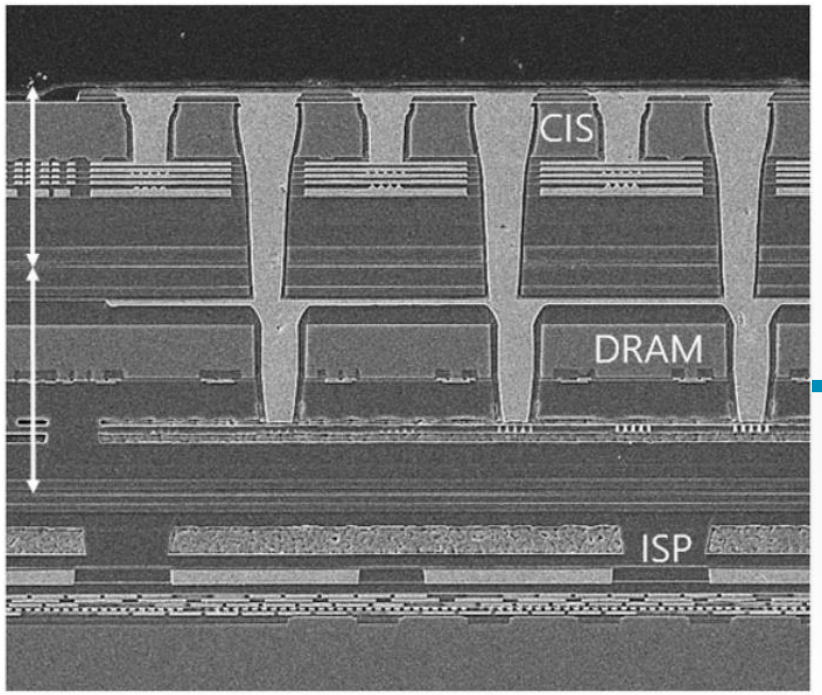
3D-SoC with wafer bonding

90nm
CIS

30nm
DRAM

40nm
logic



19.3MP @ 1/120 second
960 fps movie mode
Roadmap to per-pixel (~1um)

Impact and Design Guideline of Monolithic 3-D IC at the 7-nm Technology Node

Kyungwook Chang, Kartik Acharya, Saurabh Sinha, Brian Cline, Greg Yeric, and Sung Kyu Lim, *Senior Member, IEEE*

***Abstract*— Monolithic 3-D (M3D) IC is one of the potential technologies to break through the challenges of continued circuit power and performance scaling. In this paper, for the first time, we demonstrate the power benefits of M3D and present design guideline in a 7-nm FinFET technology node. The predictive 7-nm process design kit (PDK) and the standard cell library using both high-performance (HP) and low-standby-power (LSTP) device technologies are developed based on NanGate 45-nm PDK using accurate dimensional, material, and electrical parameters from publications and a commercial-grade tool flow. We implement full-chip M3D designs utilizing industry-standard physical design tools, and gauge the impact of M3D technology on performance, power, and area metrics. We also provide the design guidelines as well as a new partitioning methodology to improve M3D design quality. This paper shows that M3D designs outperform 2-D counterparts by 16% and 16.5% on average in terms of isoperformance total power reduction with 7-nm HP and LSTP cell library, respectively. This demonstrates the power benefits of M3D technology in both HP and low-power future generation devices.**

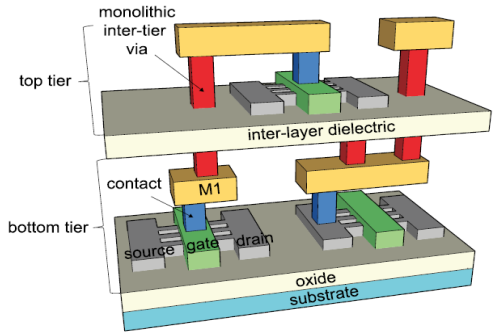


Fig. 1. Structure of M3D IC based on FinFET transistors.

GEMINI®FB XT Automated Fusion Wafer Bonding System evggroup.com

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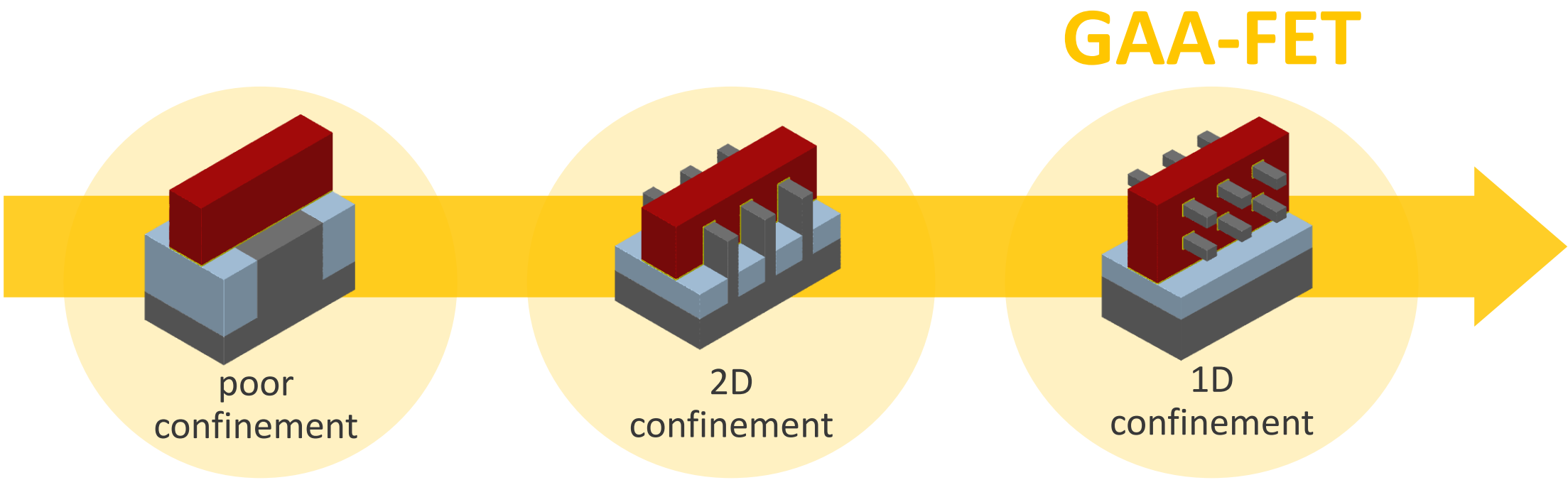
Increasing confinement in CMOS



- Enhanced mobility channel materials may improve things by 10-20%
- 5nm and 3nm will be extremely challenged to increase performance

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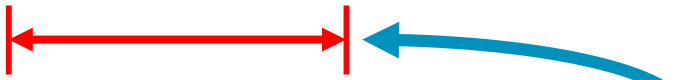
3D stacking at the transistor level

1 Moore's Law node
(just don't think about the wiring)



CMOS Inverter: 5/3nm

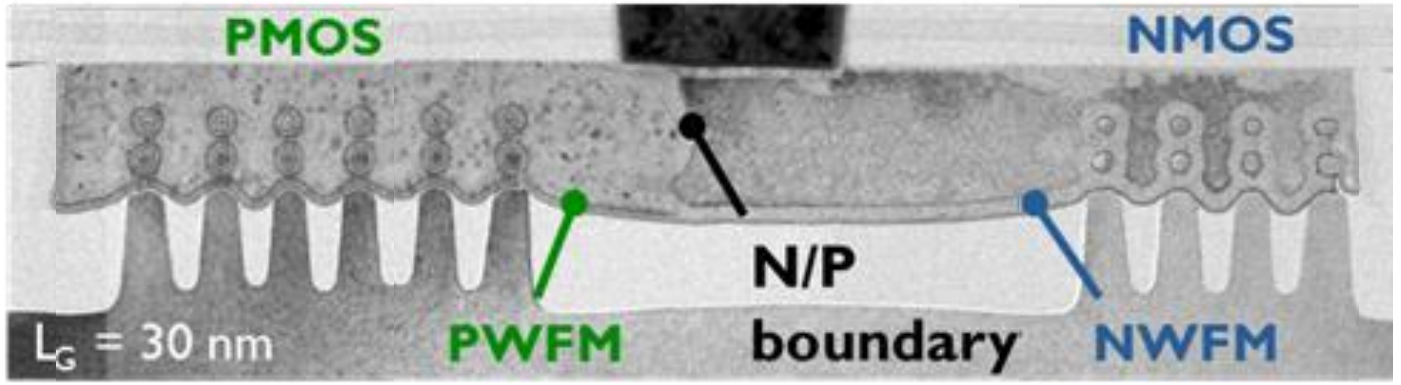


Image courtesy: imec

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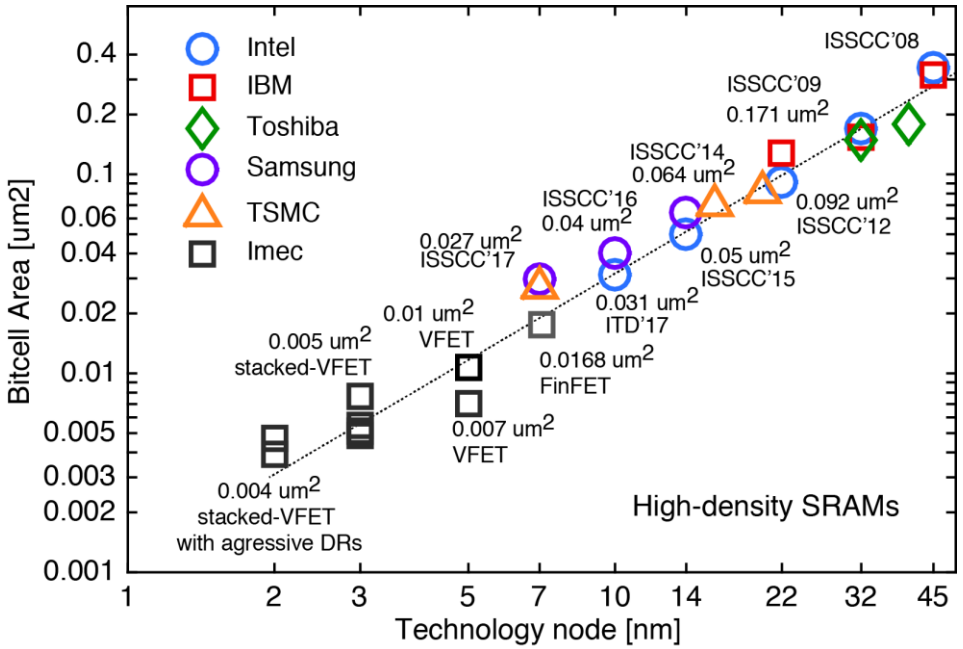
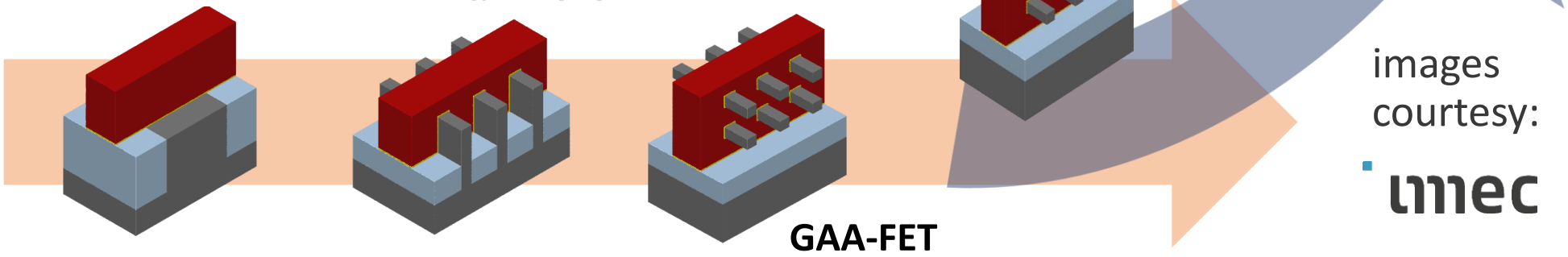
3D stacking at the transistor level





images courtesy: imec

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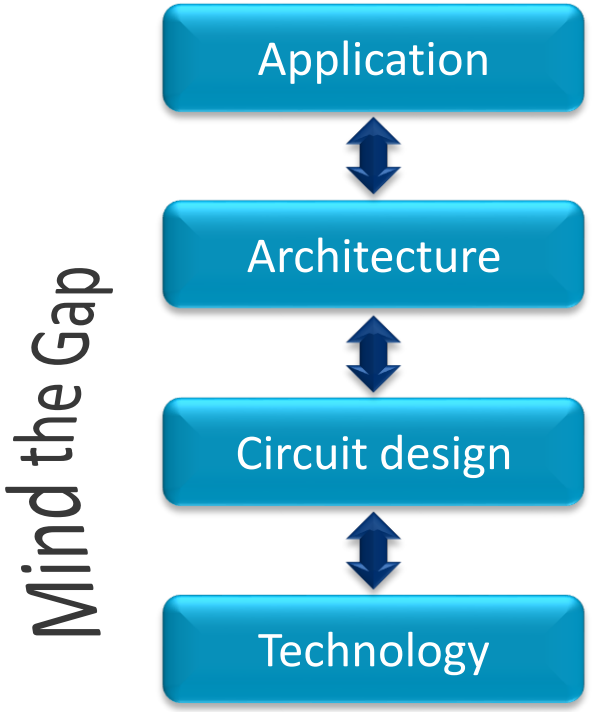
3D-SiC to 3D-SoC:

3D-IC design disrupts a large set of existing practices:

- Partitioning across 3D tiers will include signals, redistribution and power meshes, and shielding.
- This will require 3D-enablement in STA, schematic capture, PnR, DRC/LVS, PEX, and IR/EM checks, DFT / DFR, thermal and stress analysis, functional verification, assembly, yield and supply chain management



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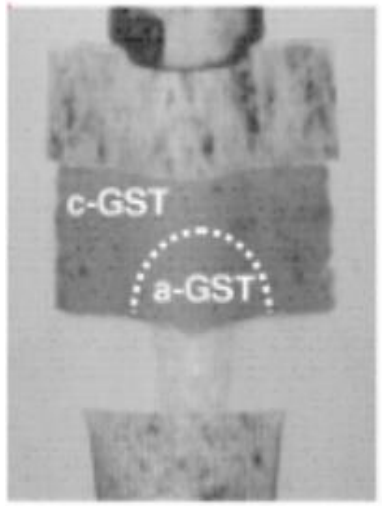
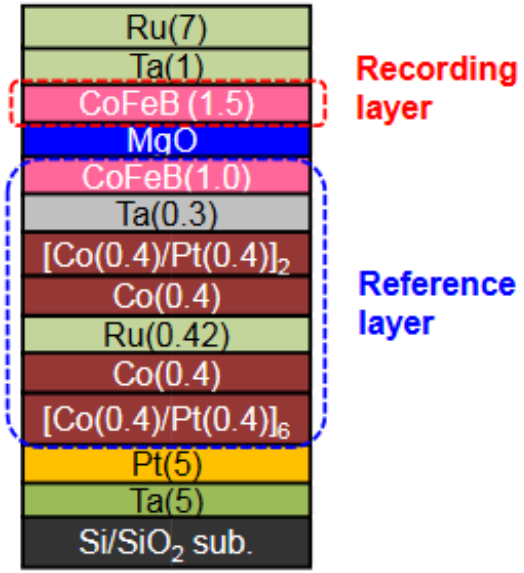
eNVM contenders: No “supermemory” … yet

- **PCM:**
  - Variability
  - Endurance



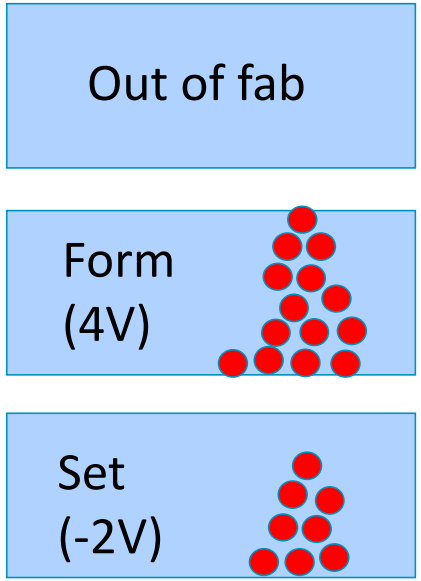
IBM

- **MRAM:**
  - Power/speed
  - Disturb
  - Cost



S. Ikeda, et al., IEDM 2014

- **Filamentary RRAM:**
  - Variability
  - Endurance
  - Scalability



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Putting it together: 3D-SoC with “e”NVM

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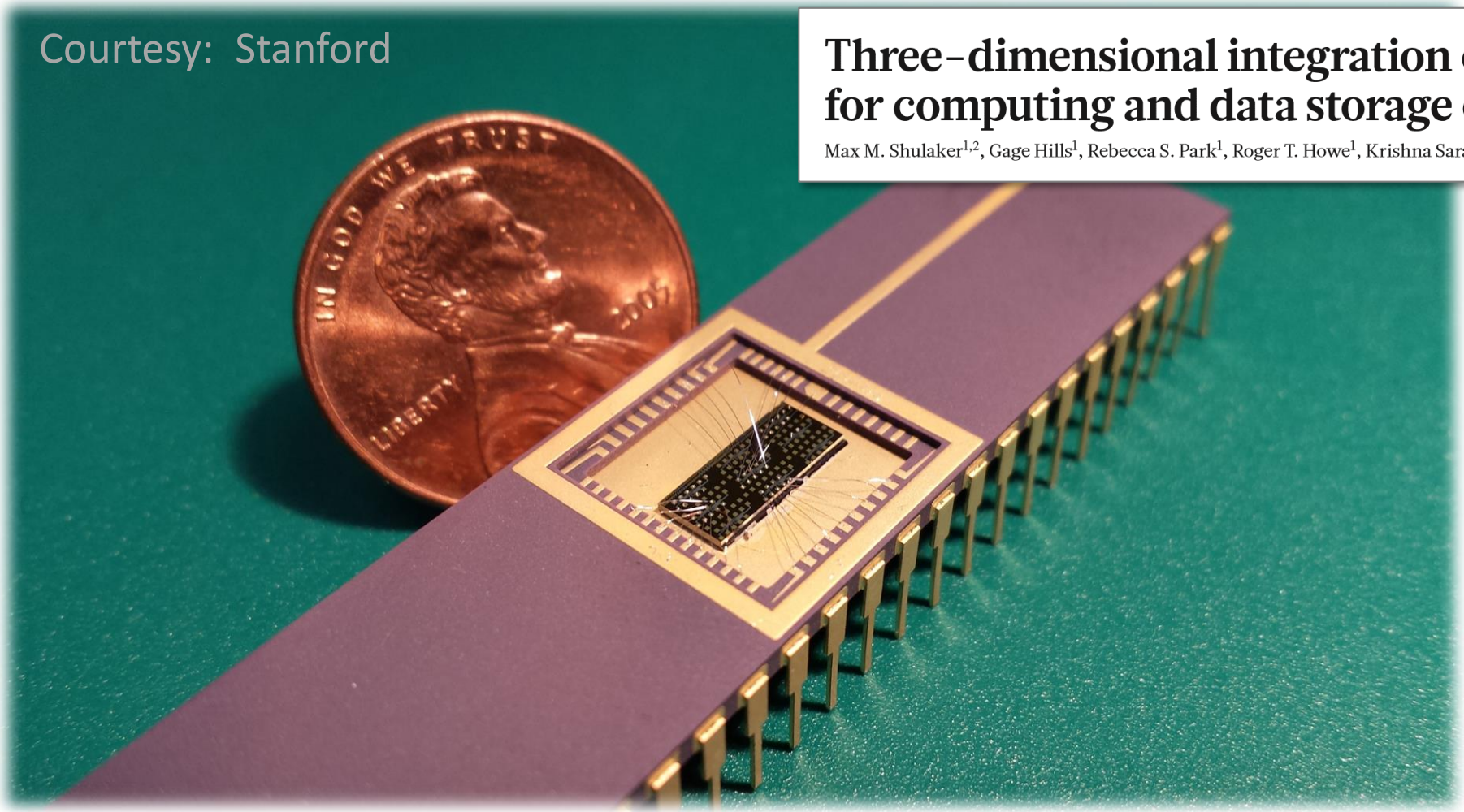

Three-dimensional integration of nanotechnologies for computing and data storage on a single chip

Max M. Shulaker[1,2], Gage Hills[1], Rebecca S. Park[1], Roger T. Howe[1], Krishna Saraswat[1], H.-S. Philip Wong[1] & Subhasish Mitra[1,3]

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Putting it together: 3D-SoC with “e”NVM

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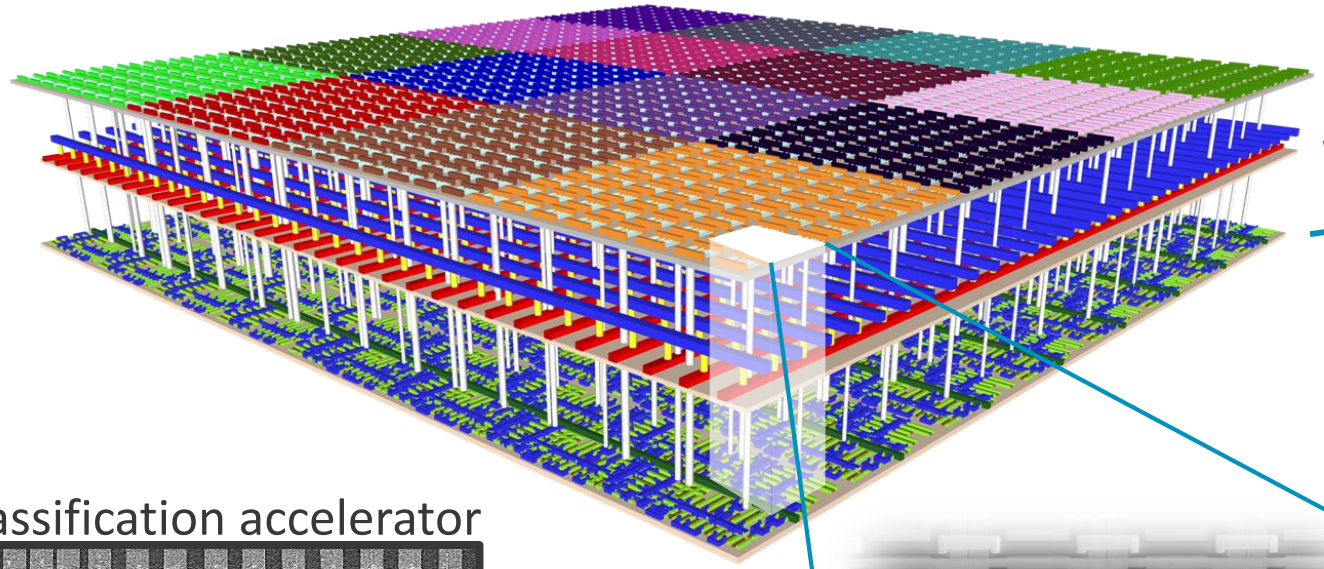
Courtesy: Stanford

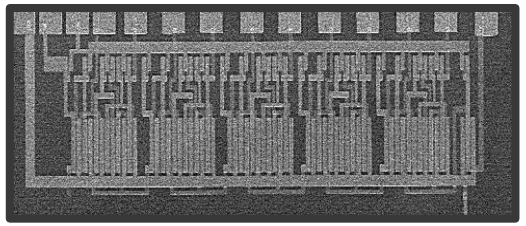


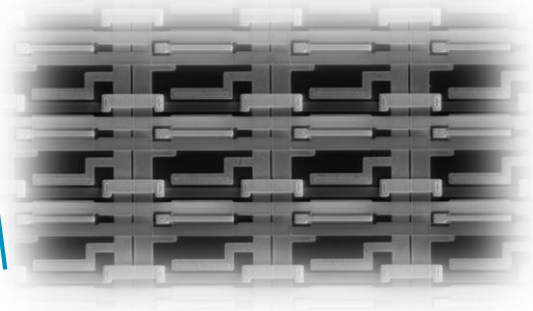
1M sensors

1Mb RRAM

2M CNT-FETs

Classification accelerator





“interwoven compute + memory + sensing”

Toward 1000x EDP, especially for data-rich applications where >85% of the clock cycles are for memory

Increasing diversity of computing, built on 2D CMOS, enabled by 3DIC

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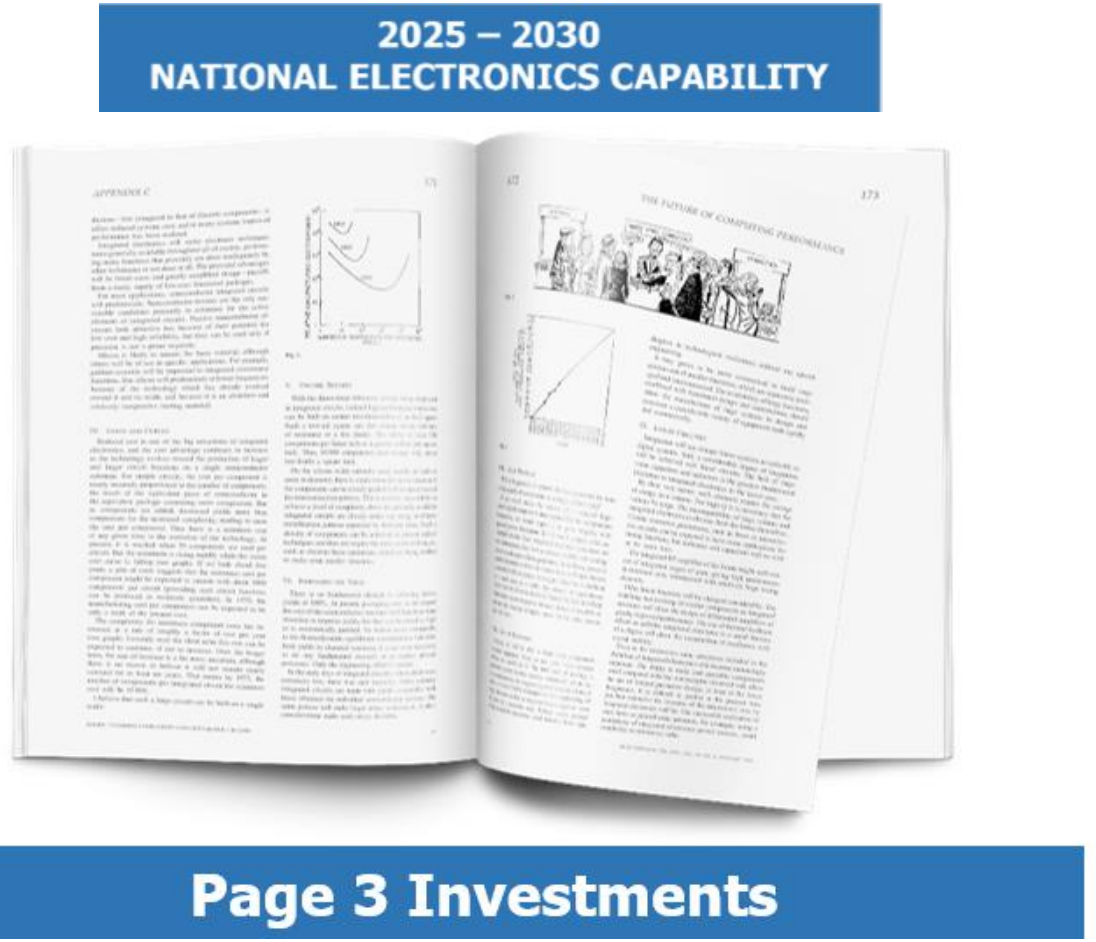
DARPA's Electronics Resurgence Initiative

"Page 3 investments"

3DIC + NVM intra-layer capabilities:
9M interconnects/mm^2, 50Tb/s, 2pJ/bit.

Demonstrator goals:

- 50X performance at power compared with 7nm 2D CMOS
- 4GB NVM and 50M logic gates 200mm2
- Cost comparable to equivalent 2D CMOS



https://www.darpa.mil/work-with-us/electronics-resurgence-initiative

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“I thought this guy was going to talk about 20-30 years out?”

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DARPA's Electronics Resurgence Initiative

"Page 3 investments"

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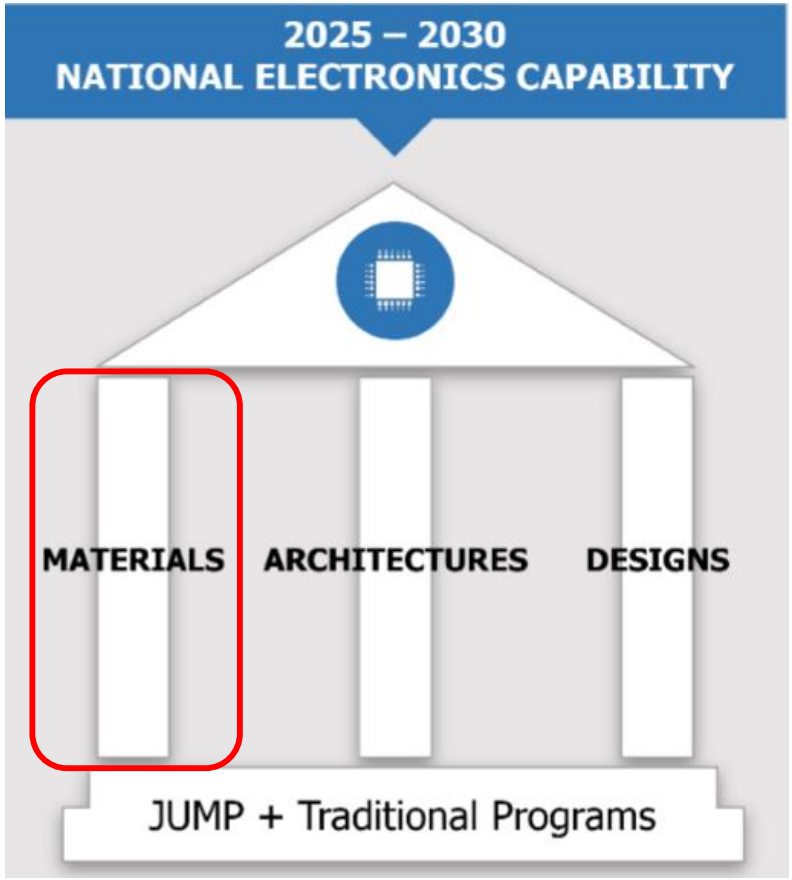

https://www.darpa.mil/work-with-us/electronics-resurgence-initiative

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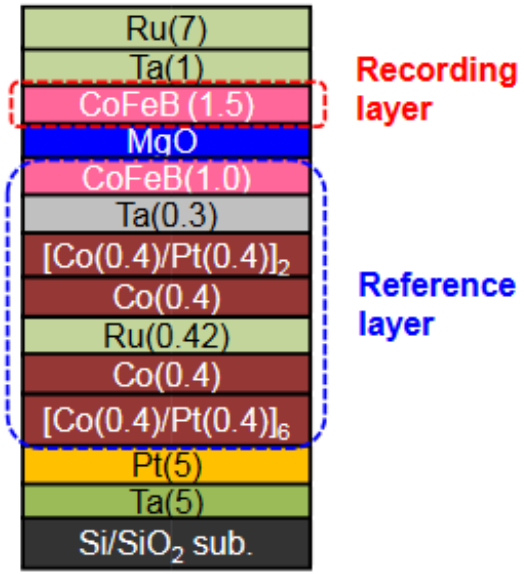
Representative “new material” timeline:

~30 years discovery to product



2017 eMRAM samples from foundries
2018 eMRAM product for use

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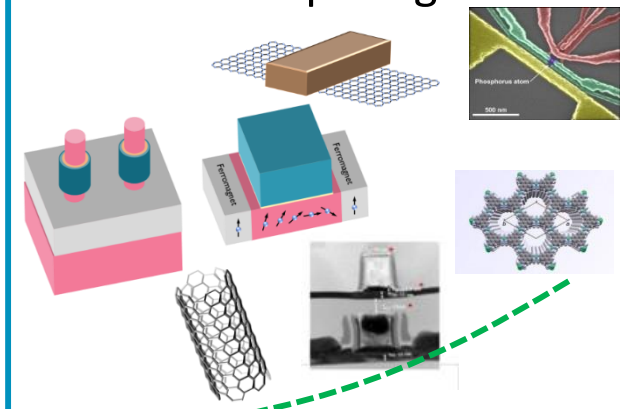
Future technology pipeline

Needs:

- Extend conventional CMOS scaling
- Accelerate device and materials R&D from suppliers, consortia and universities
  - Proper benchmarking, relevant demonstrators
- Manage unprecedented diversity and change

Researchers:
Reboot Computing



Foundries
Extend Moore's Law

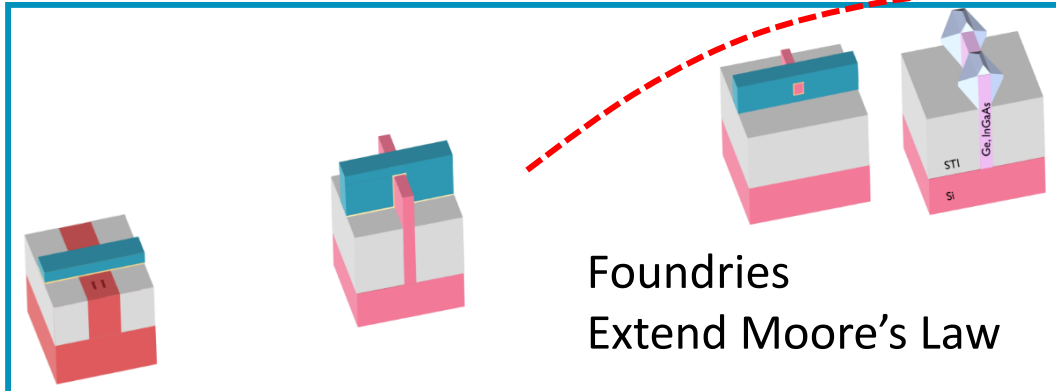


Figure of Merit

1971 2010 2015 2020 2025

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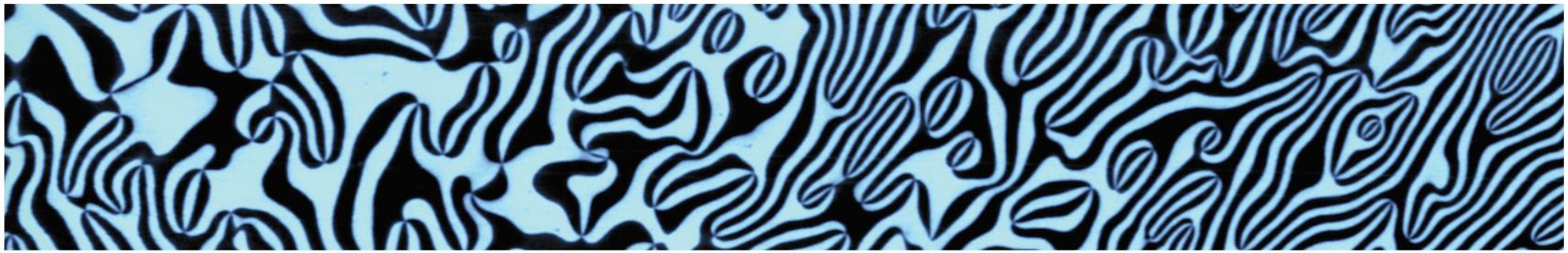

Piezoresponse force microscopy image of the ferroelectric domain structure of multiferroic $ErMnO_3$. The dark and light regions correspond to opposite orientations of the electric dipoles. The vertical dimension is about 20 µm. Image courtesy of Manfred Fiebig and Martin Lilienblum (ETH Zürich)

erbium manganate

Fundamental Materials Research and the Course of Human Civilization

Nicola Spaldin*

Unless we change direction, we are likely to wind up where we are headed.
(Ancient Chinese proverb)

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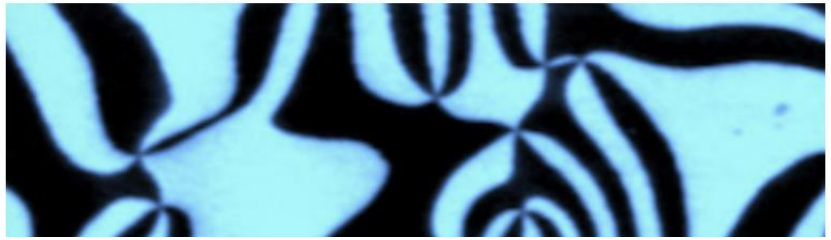
How Materials Science Will Determine the Future of Human Civilization

MIT Technology Review

by Emerging Technology from the arXiv August 16, 2017

Why Moore's law is set to destroy the planet and how to stop it

September 19, 2017



FUTURIST

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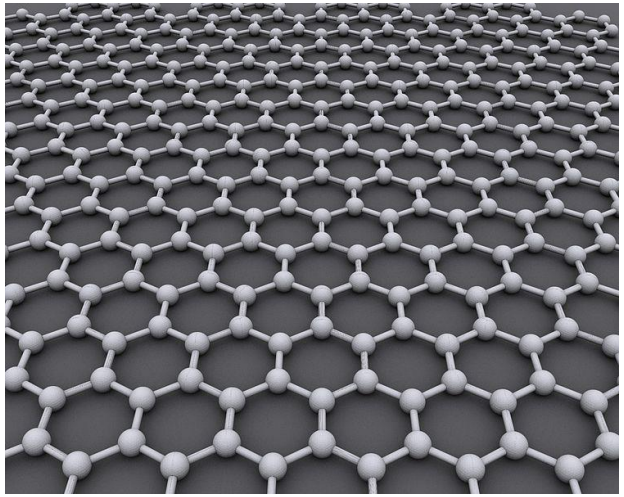
Materials innovation: 2D (graphene)

Andre Geim

Konstantin Novoselov



2004: + = 2010 Nobel Prize

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Materials revolution snapshot: 2D

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Materials revolution snapshot: 2D

IEEE SPECTRUM

The Most Complex 2D Microchip Yet

By Charles Q. Choi
Posted 11 Apr 2017 | 16:30 GMT

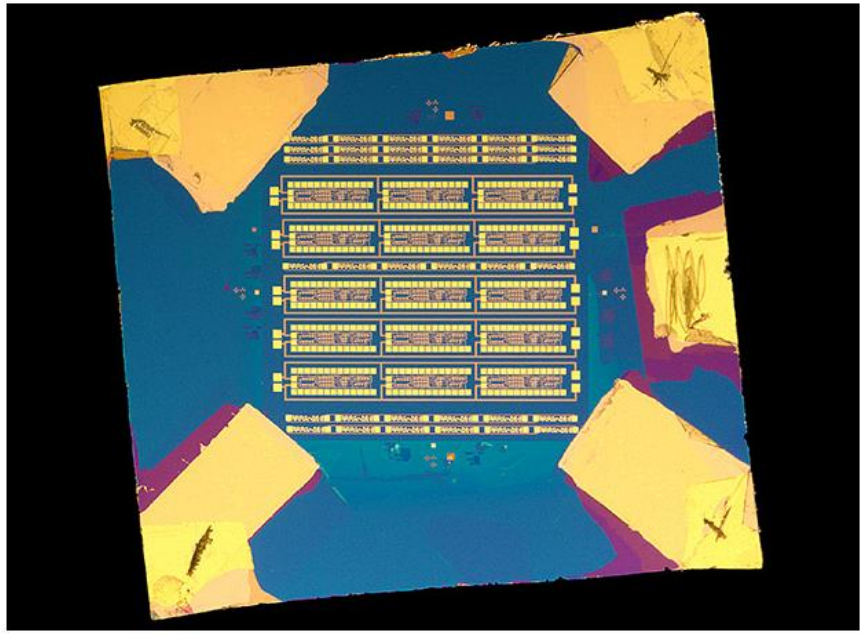

Image credit: Photo: Stefan Wachter

200 molybdenum disulfide transistors (MoS_2FETs)

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Materials revolution snapshot: 2D

Journal of Materials Science: Materials in Electronics

pp 1–6

High-performance transparent ultraviolet photodetector based on thermally reduced graphene oxide and ZnO thin films

Authors | Authors and affiliations

A. M. Bazargan, F. Sharif, S. Mazinani, N. Naderi

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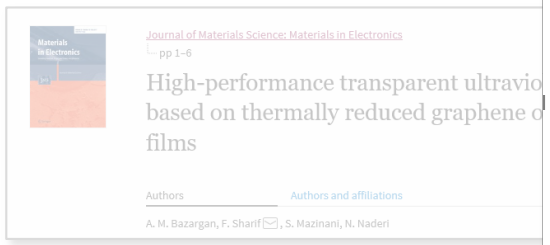
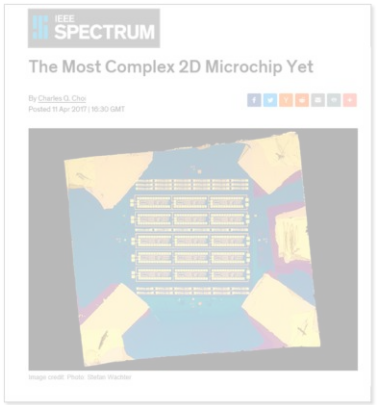
Materials revolution snapshot: 2D



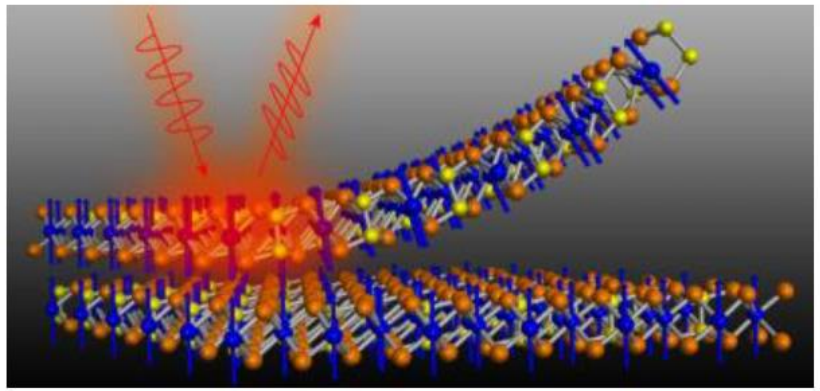


Graphene-info THE GRAPHENE EXPERTS

Researchers discover a magnetic 2D material

Apr 30, 2017 **2D materials** **Magnetism** **Technical / Research**

Researchers from the Lawrence Berkeley National Laboratory discovered the world's first magnetic 2D material - chromium germanium telluride (CGT). It was debatable whether magnetism could survive in such thin materials - and this discovery could pave the way to extremely thin spintronics devices.



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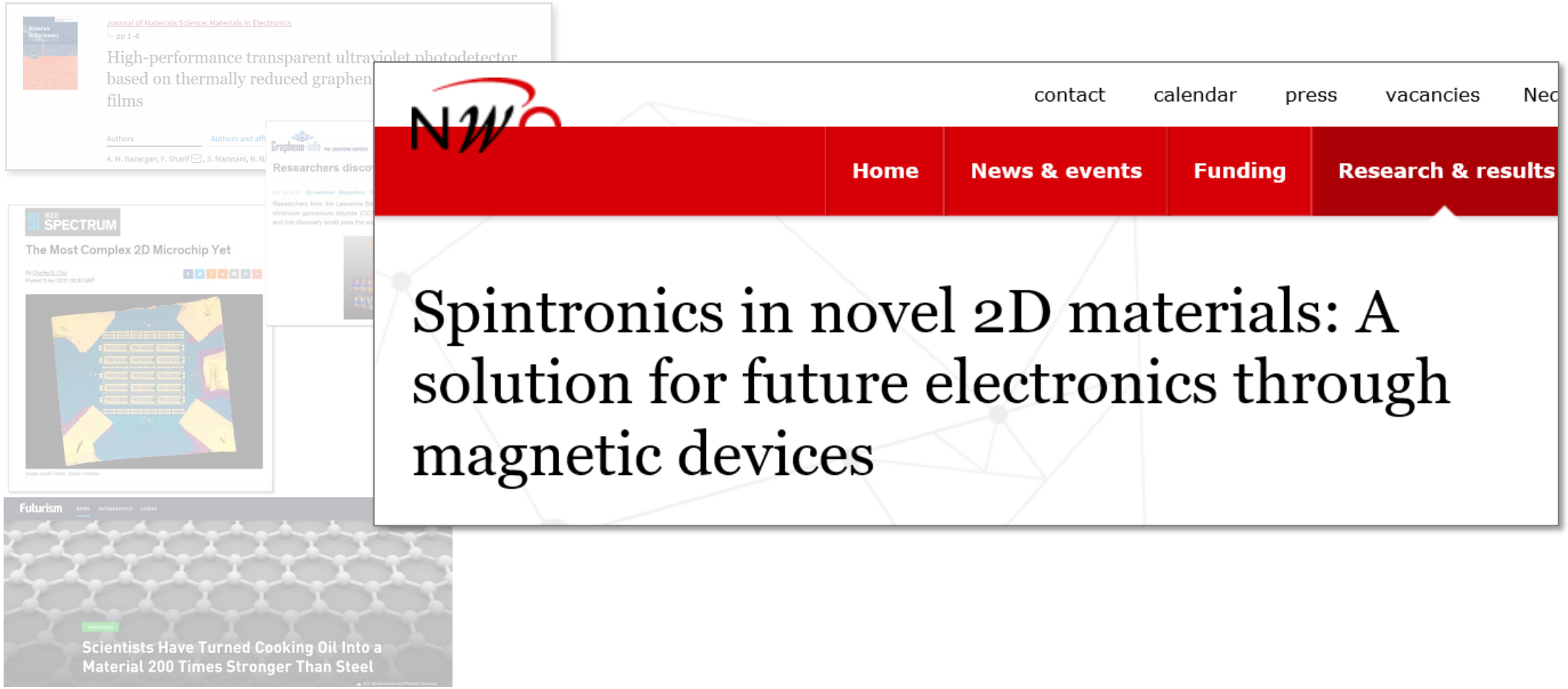
Materials revolution snapshot: 2D



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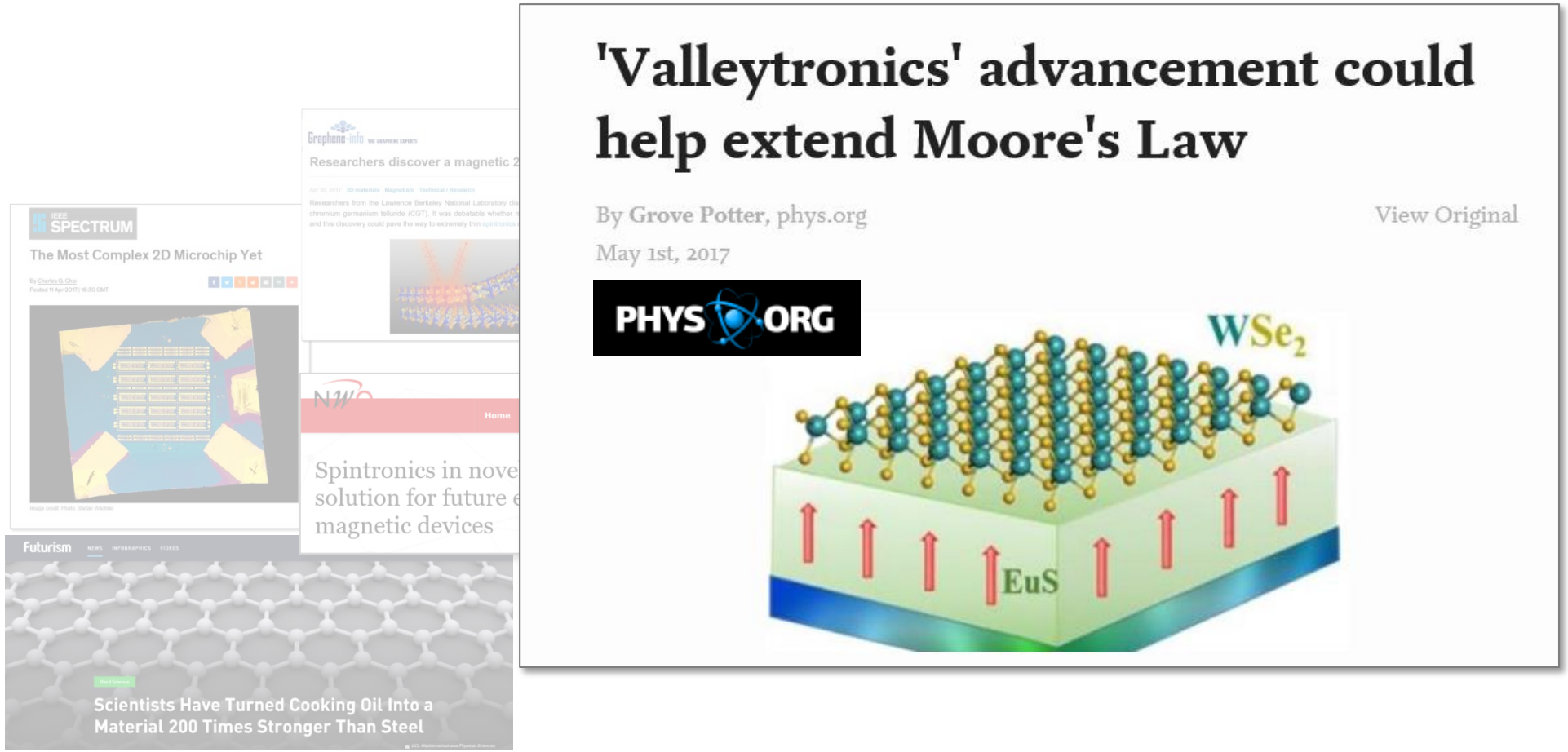
Materials revolution snapshot: 2D



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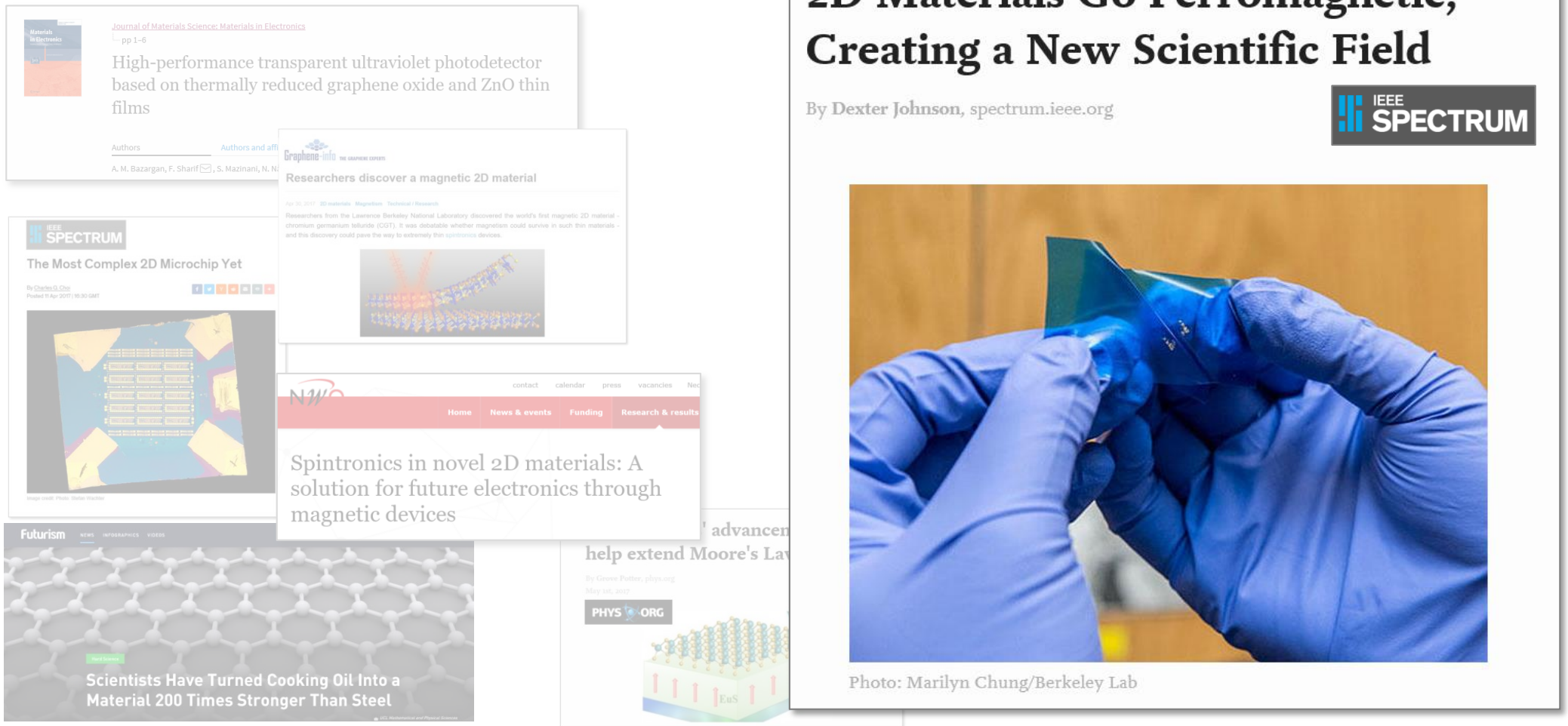
Materials revolution snapshot: 2D



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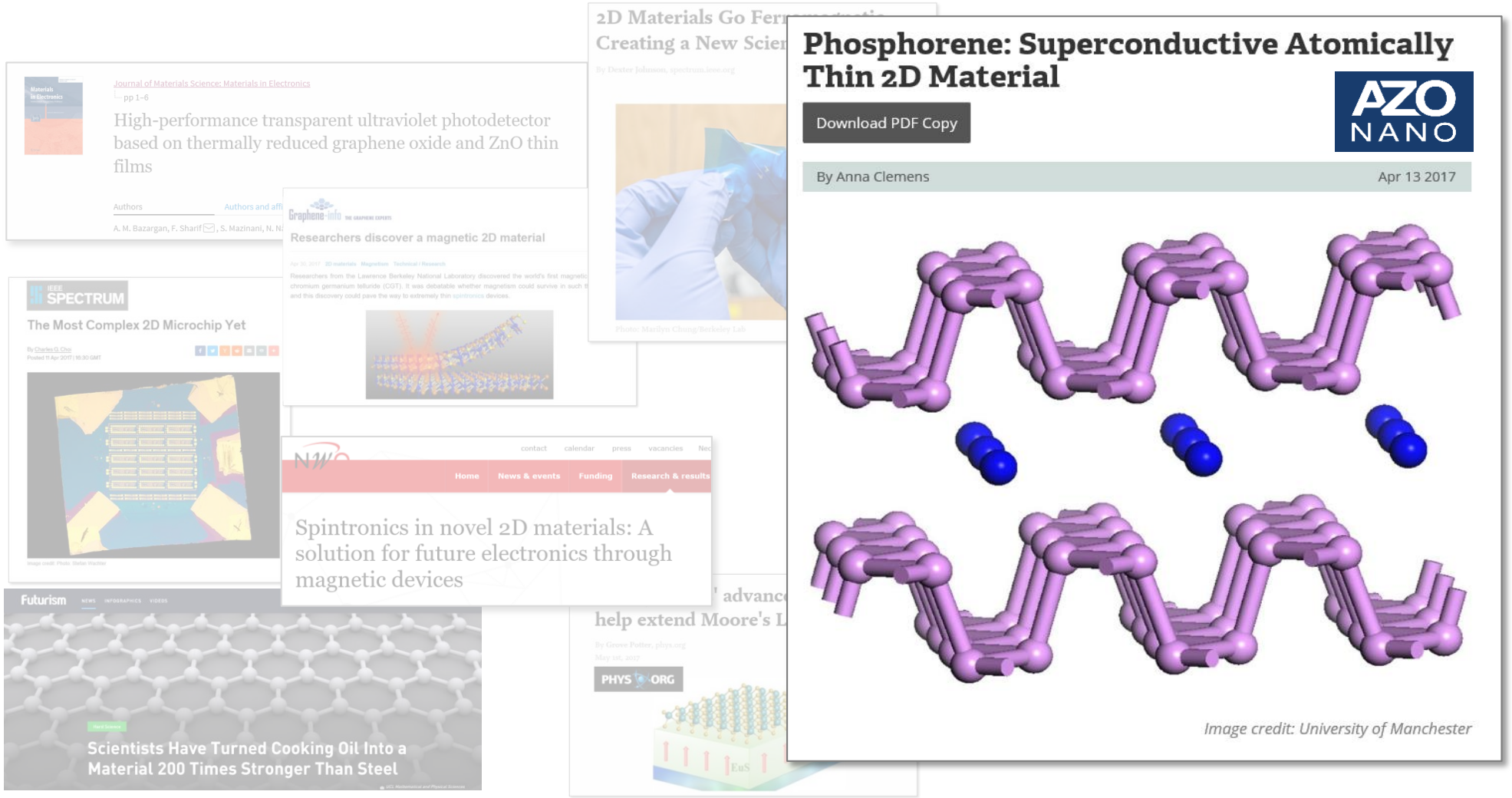

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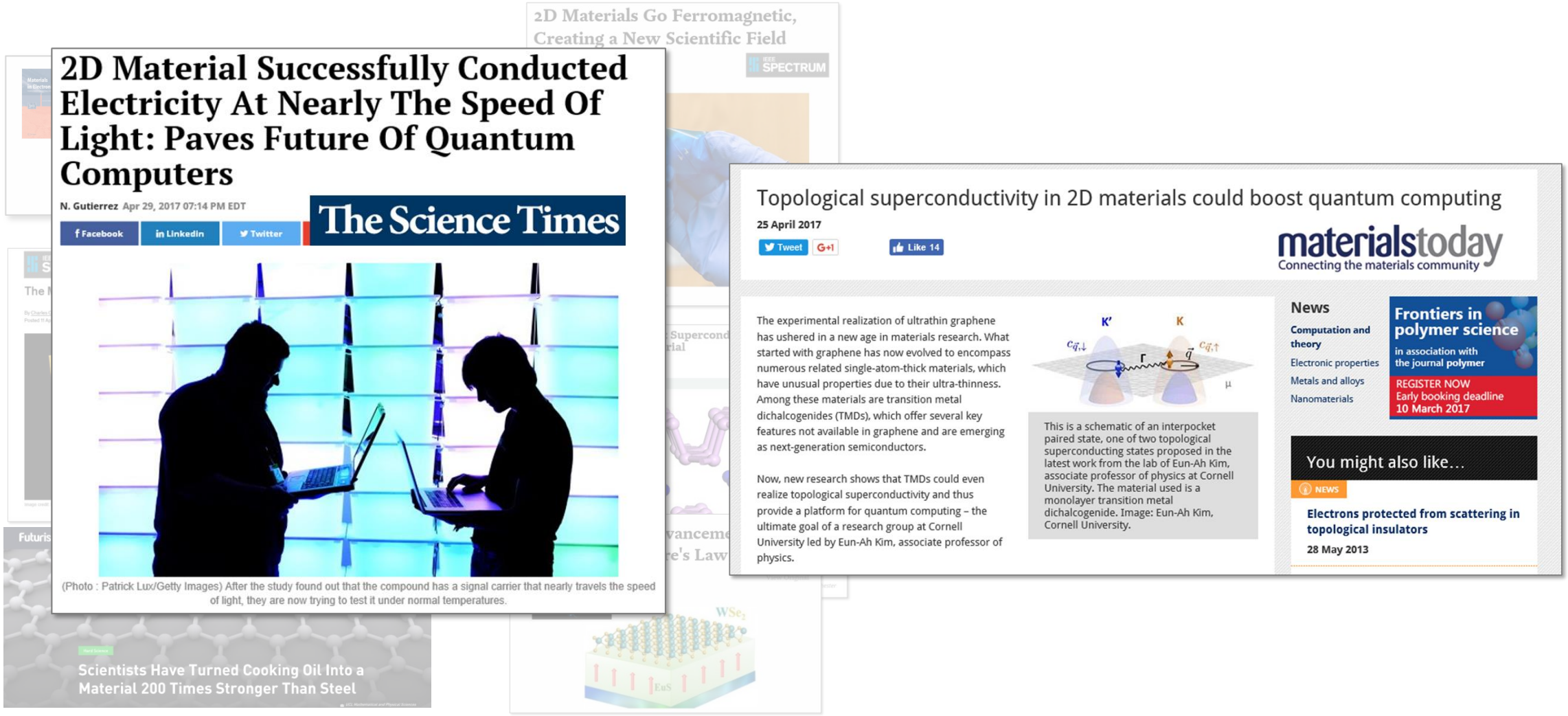

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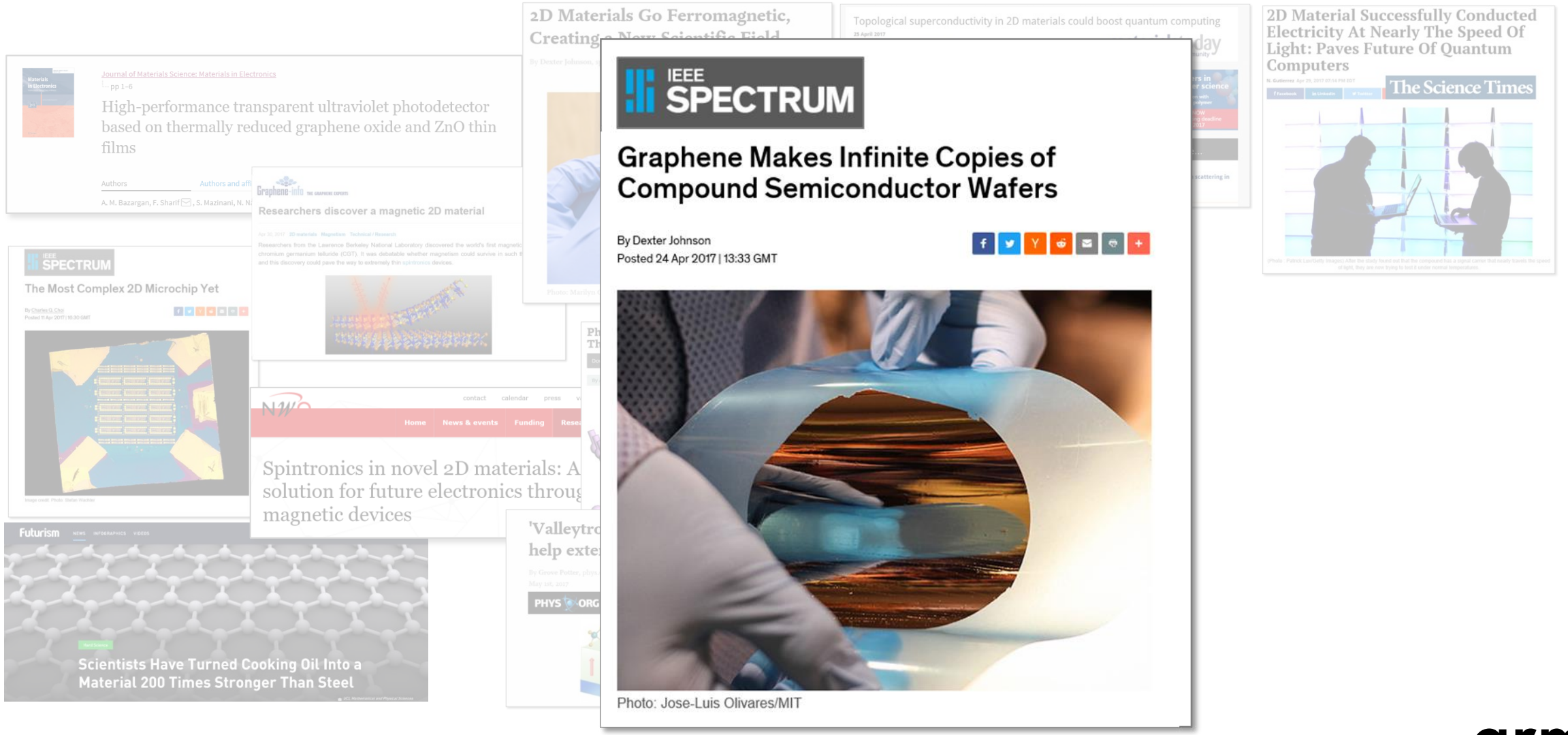

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Materials revolution snapshot: 2D

2D Materials Go Ferromagnetic,

Topological superconductivity in 2D materials could boost quantum computing

2D Material Successfully Conducted
he Speed Of
Quantum

cience Times

Journal of Materials Science: Materials in
pp 1–6

High-performance
based on thermally
films

Authors

A. M. Bazargan, F. Sharif, S. Mazinani,

IEEE SPECTRUM

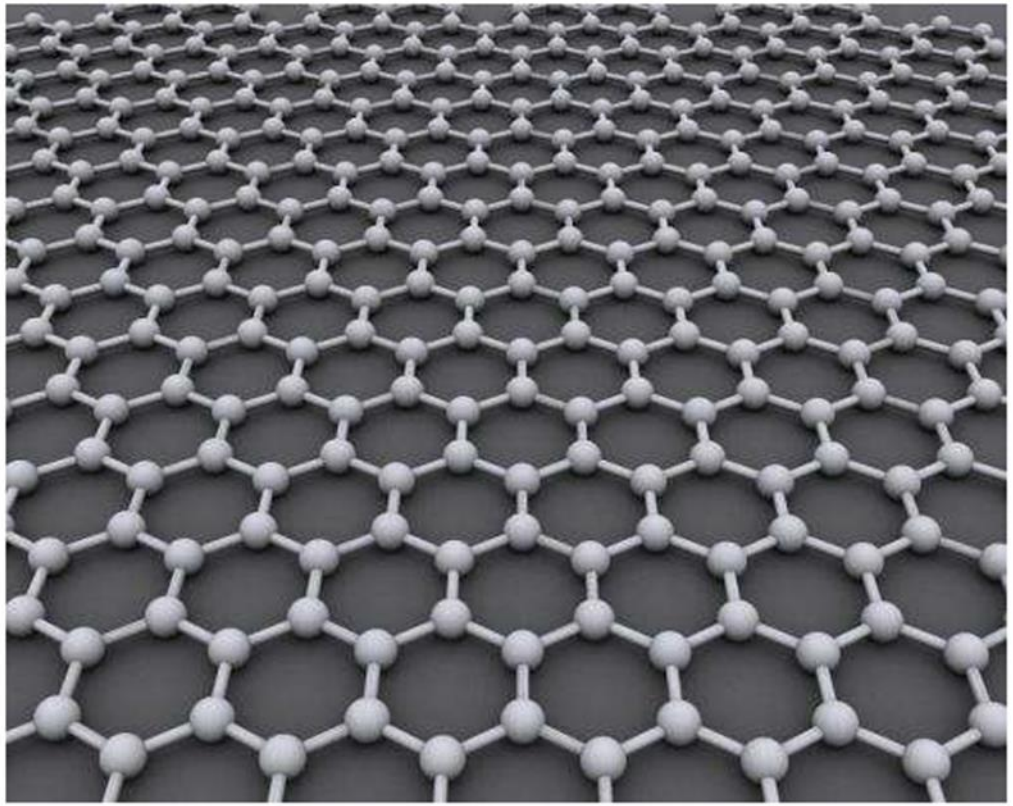
The Most Complex 2D Microchip Yet

Futurism NEWS INFOGRAPHICS VIDEOS

Scientists Have Turned
Material 200 Times Str

Graphene coating that changes color when deformed or cracked

April 10, 2017 by Bob Yirka report



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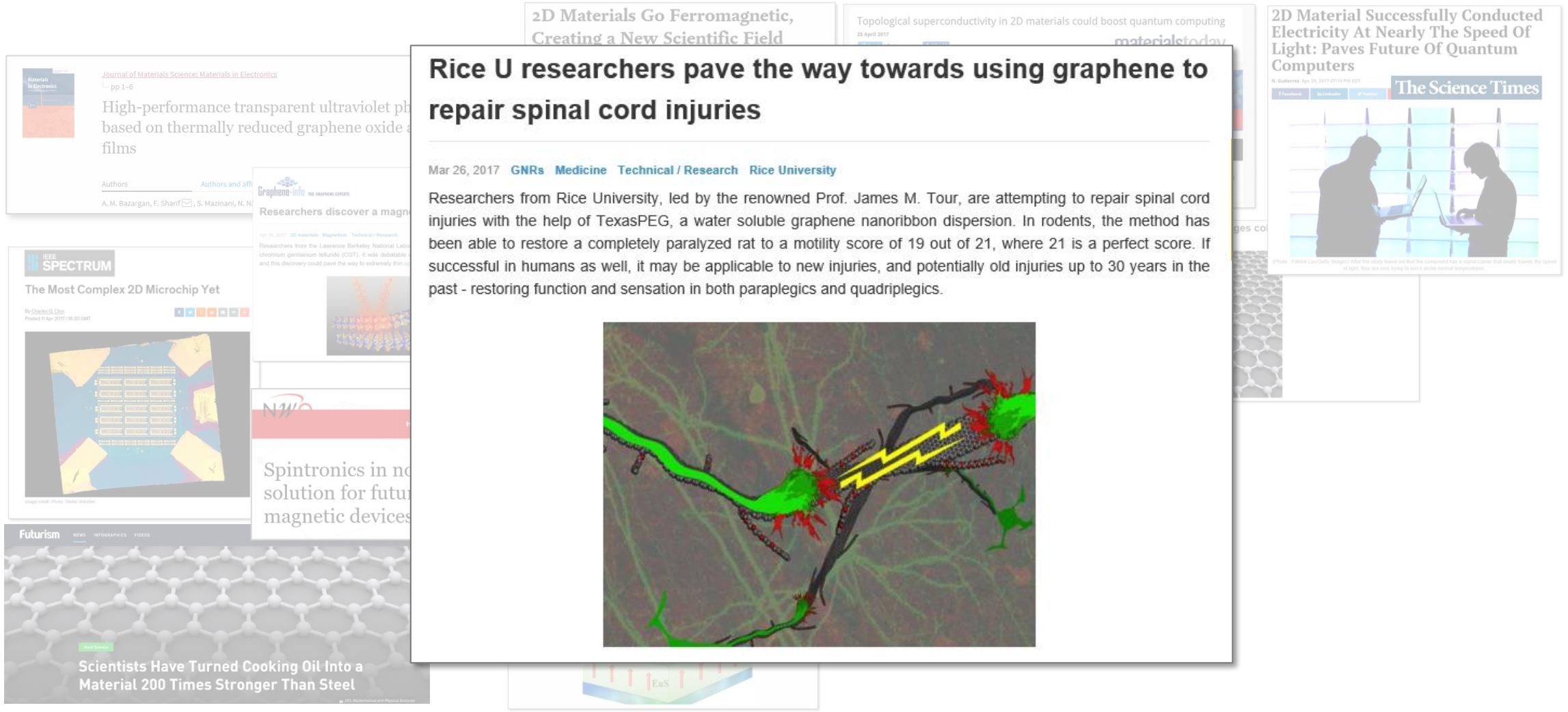

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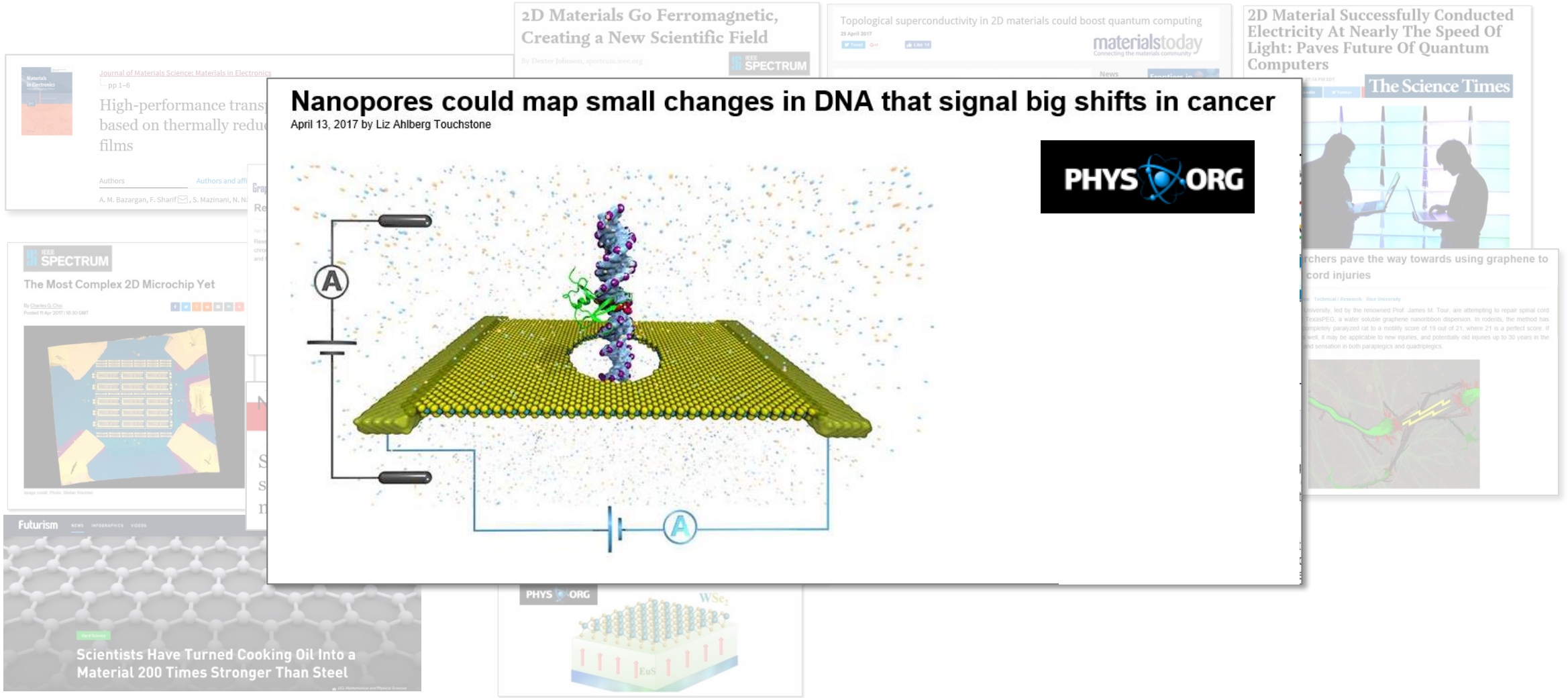

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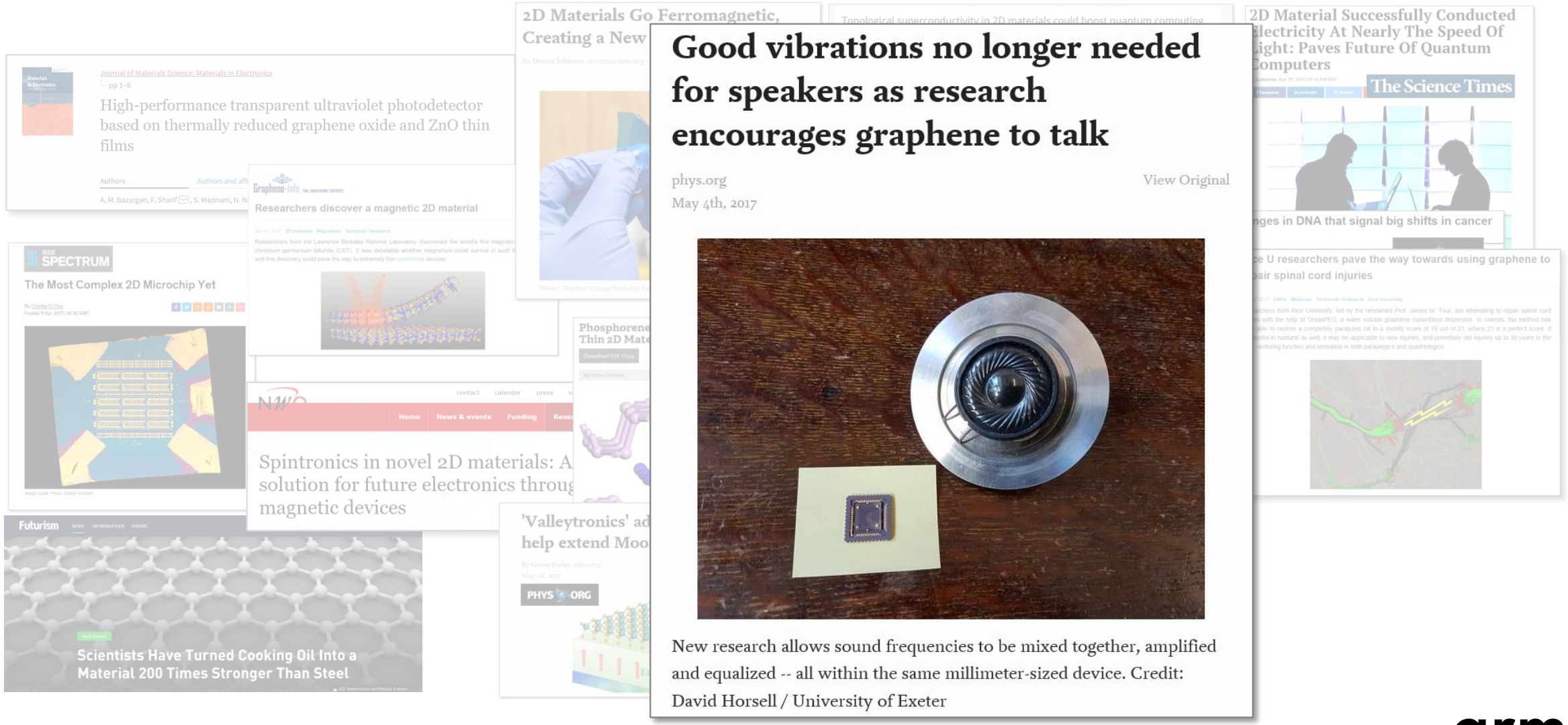

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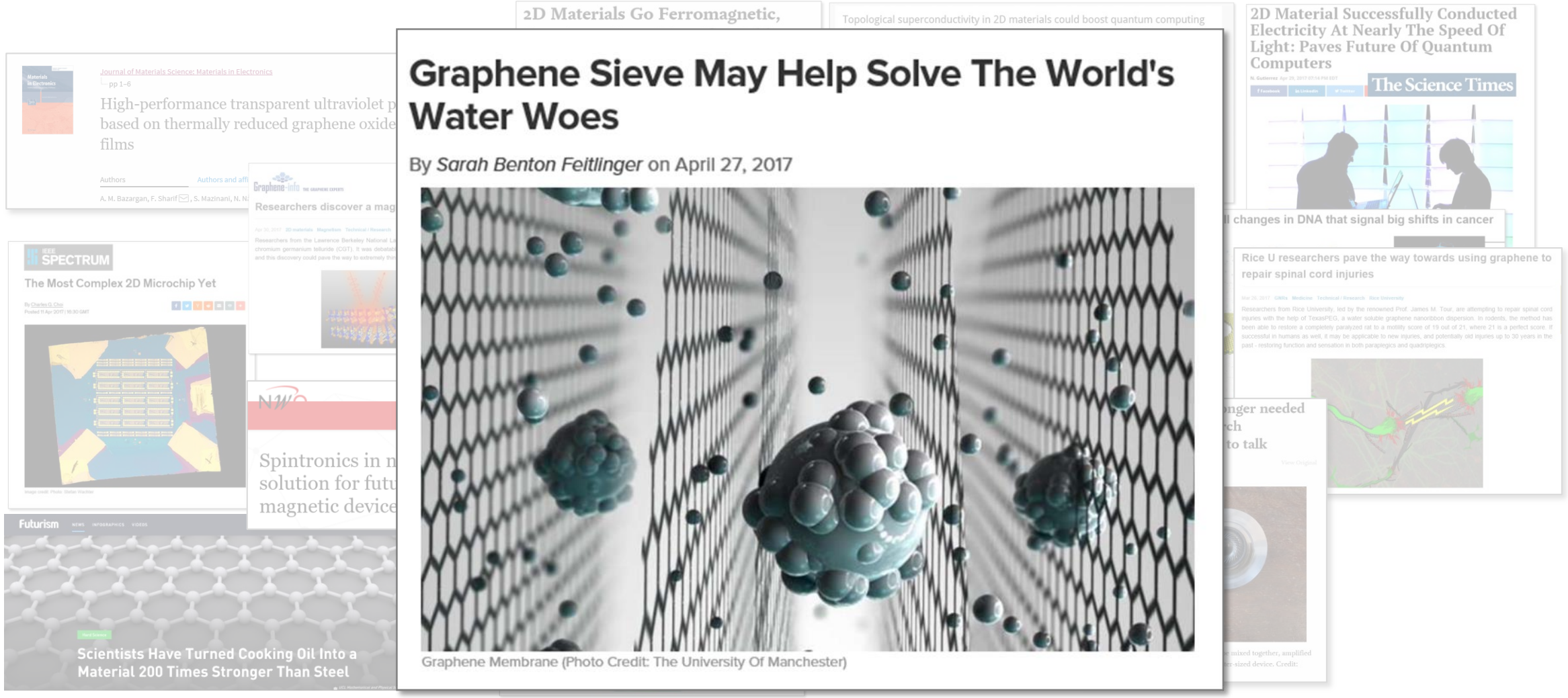

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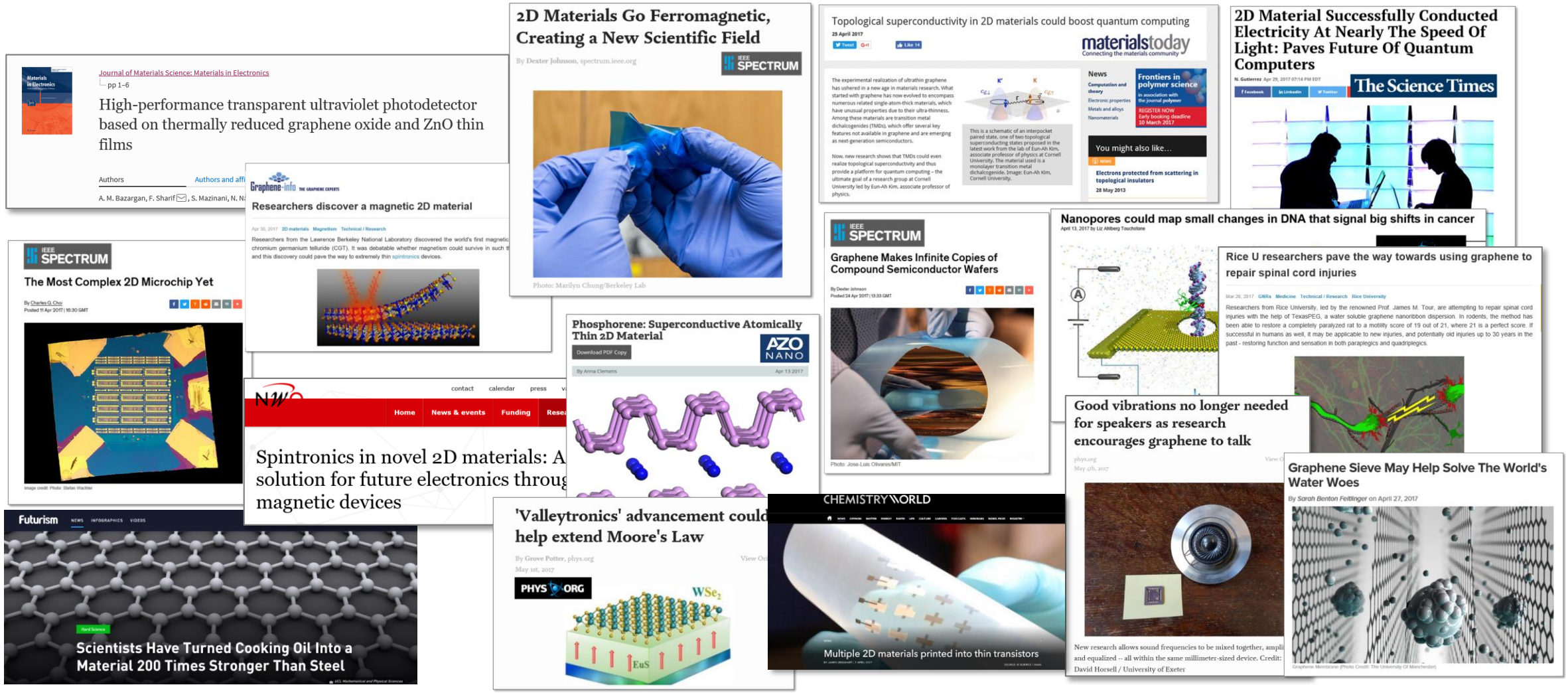
All of these 2D materials news items came in a 3-4 week span



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Future technology pipeline

Needs:

- Extend conventional CMOS scaling
- Accelerate device and materials R&D from suppliers, consortia and universities
  - Proper benchmarking, relevant demonstrators
- Manage unprecedented diversity and change

Researchers:
Reboot Computing

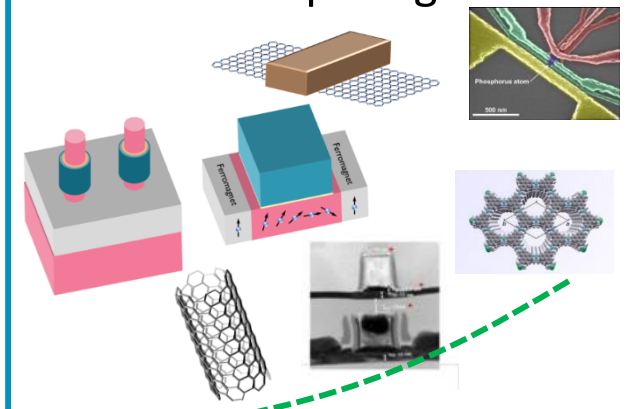
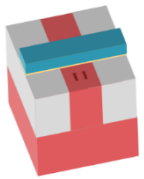
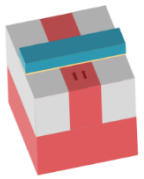
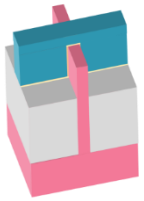
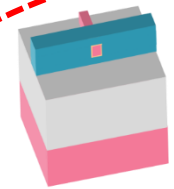


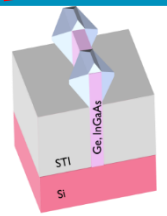
Figure of Merit











Foundries
Extend Moore's Law

1971 2010 2015 2020 2025

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Summary: system scaling opportunity is out there

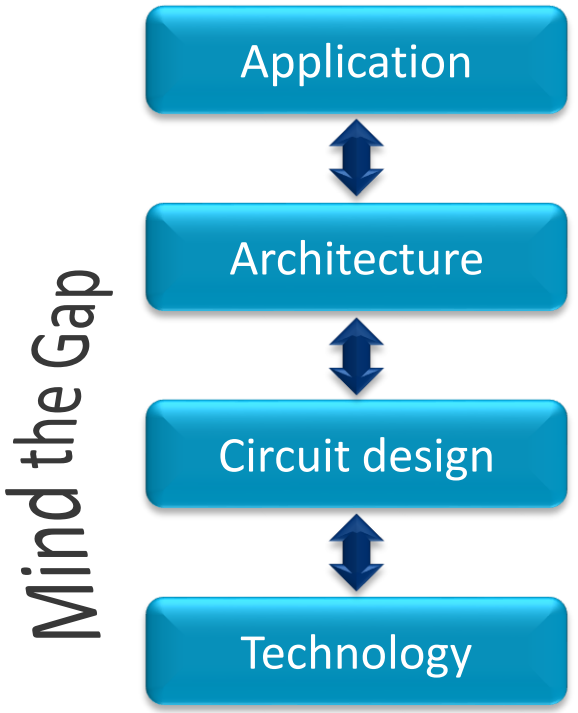
The (easy) path of pitch scaling is waning

New knobs are coming to the masses:
3D-SiC → 3D-SoC → 3D-IC and novel memories

New materials will enable an explosion of computing options, from efficient memory and I/O, to low cost IoT enablers.

Industry challenge:

Stem the slowing of “Moore’s Law” just long enough, while also accelerating novel devices enabled by entirely new materials, and manage all of this diversity and change.



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Thank You

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A word of caution on cost prediction math

7nm steppers are 50% faster than 28nm steppers

> 250 wafers per hour = < 15 seconds per wafer

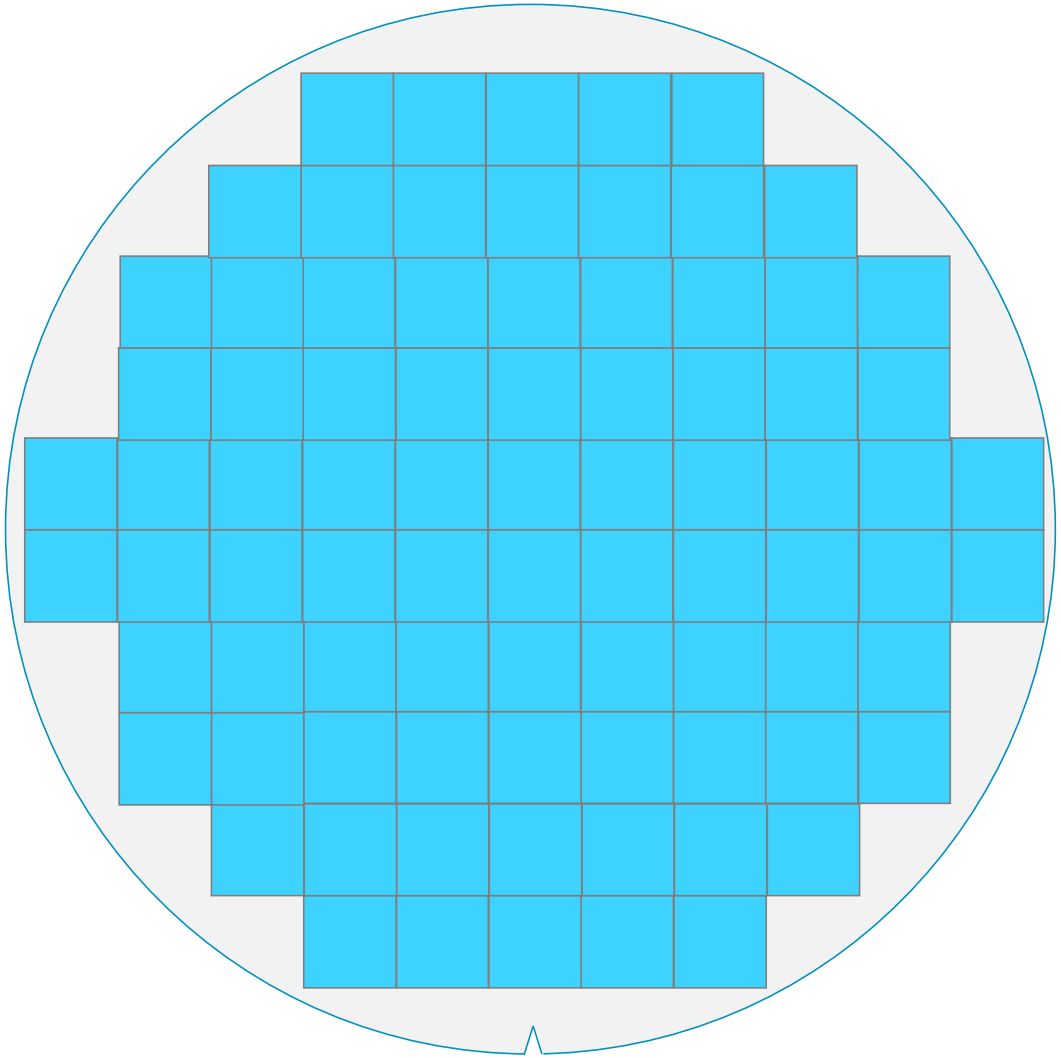
Chuck moves > 1m/second (develops >10G)

3 nm X and Y accuracy*

*drop England onto the globe, align it to a precision of one brick, 5 times per second

are your circuits worthy?

Continuous improvement from all suppliers: resist, light source, mask, etch….



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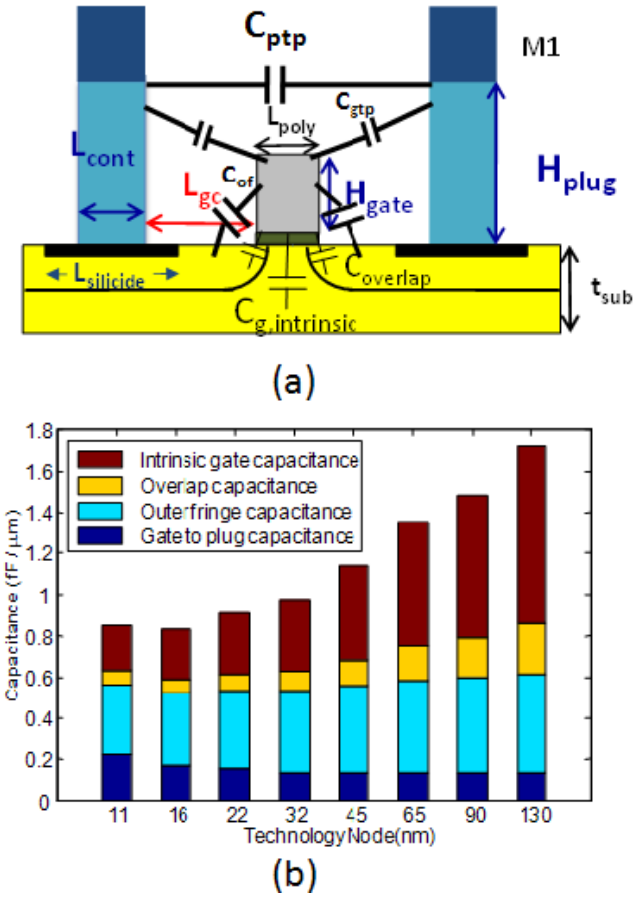
Moore has a better story than Dennard



HS Wong, et al., SISPAD 2009

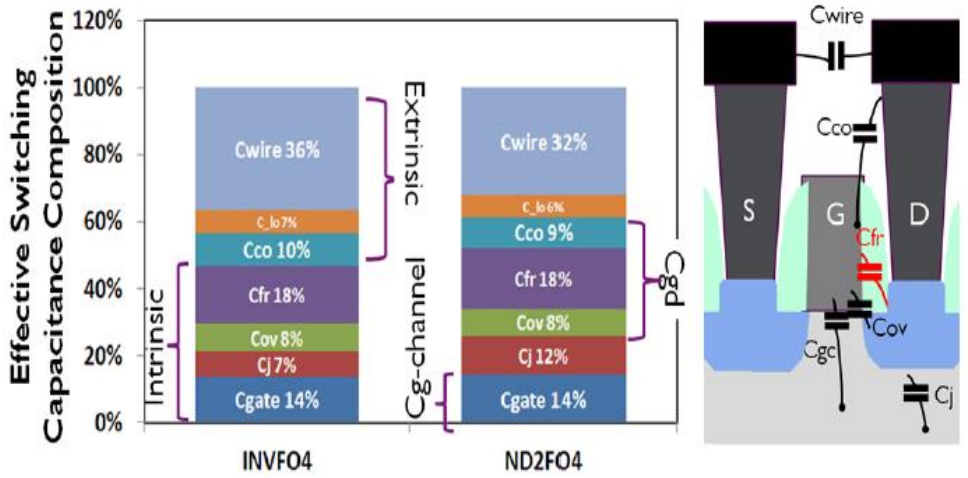


Fig. 6. Breakdown of intrinsic & extrinsic switching capacitances for typical post-28nn simple logic gates (INV and NAND), post-layout parasitic extraction and simulated witl SPICE.

IMEC: IEDM 2013

Today:

we want to scale L_G in order to open up more contact area

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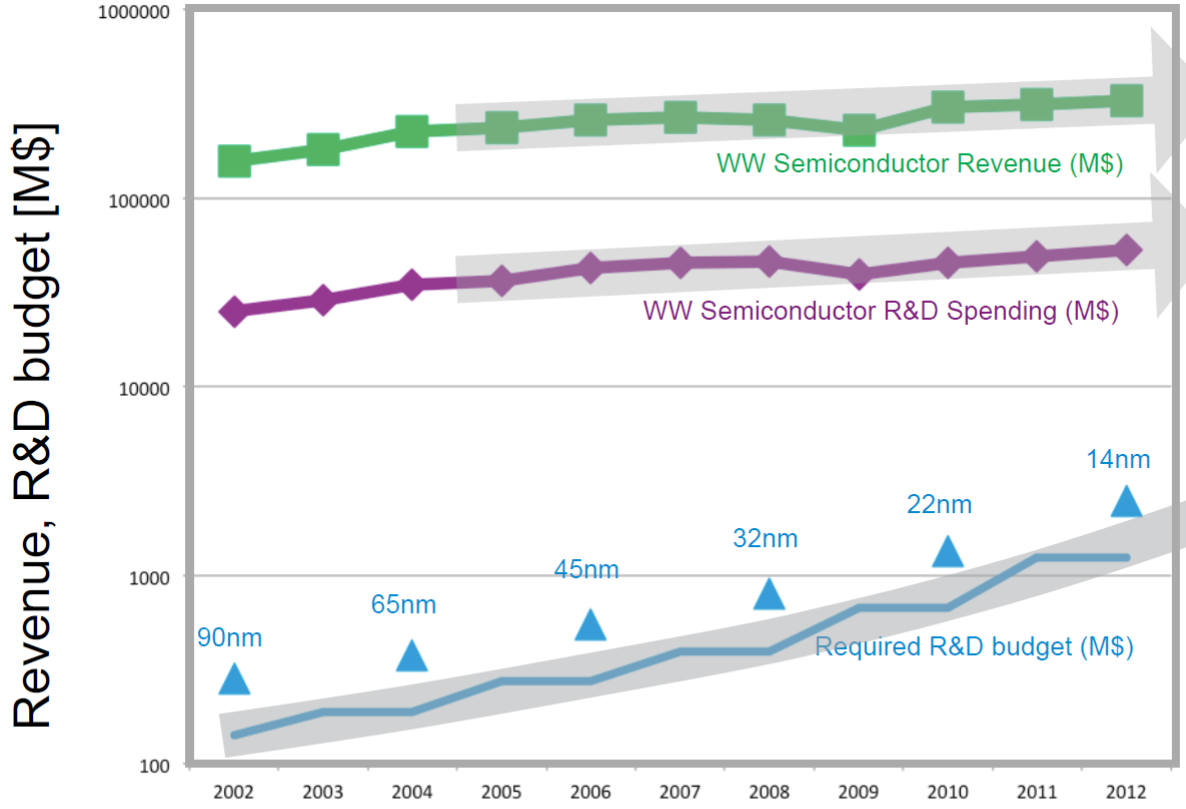
Pressure on R&D costs



http://theconfab.com/wp-content/uploads/2013/07/cf13_lode_lauwers.pdf

source: IHS iSupply
Sematech Report
IBS 2011

Industry has its hands full with ≤ 5nm development.

The complexities of solutions for 3/2 nm solutions will be unprecedented

Will there be any $ left for research?

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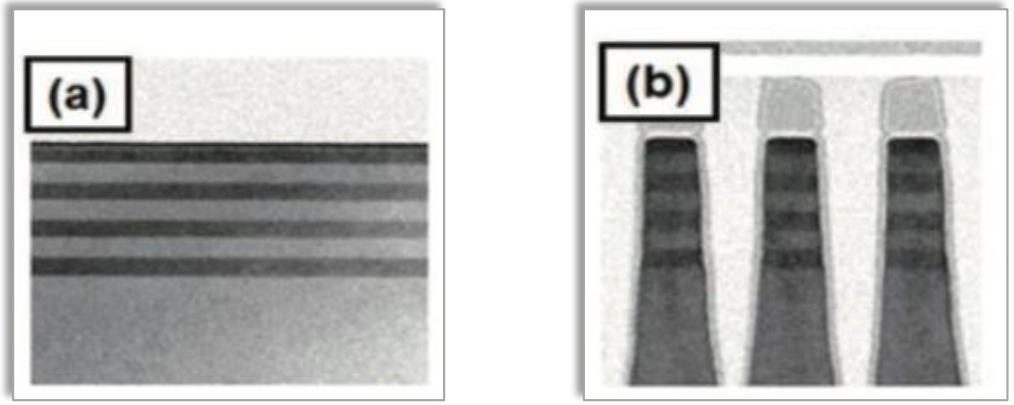
FinFET → GAA Nanosheet

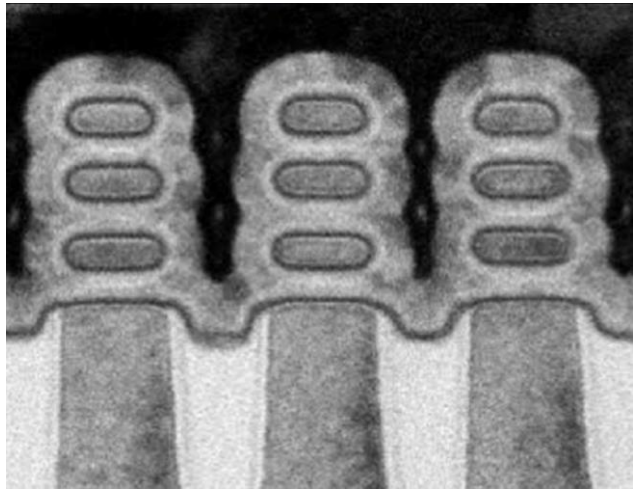
2017 VLSI TECHNOLOGY SYMPOSIUM

Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET

N. Loubet[1], T. Hook[1], P. Montanini[1], C.-W. Yeung[1], S. Kanakasabapathy[1], M. Guillorn[1], T. Yamashita[1], J. Zhang[1], X. Miao[1], J. Wang[1], A. Young[1], R. Chao[1], M. Kang[2], Z. Liu[1], S. Fan[1], B. Hamieh[1], S. Sieg[1], Y. Mignot[1], W. Xu[1], S.-C. Seo[1], J. Yoo[2], S. Mochizuki[1], M. Sankarapandian[1], O. Kwon[2], A. Carr[1], A. Greene[1], Y. Park[2], J. Frougier[3], R. Galatage[3], R. Bao[1], J. Shearer[1], R. Conti[1], H. Song[2], D. Lee[2], D. Kong[1], Y. Xu[1], A. Arceo[1], Z. Bi[1], P. Xu[1], R. Muthinti[1], J. Li[1], R. Wong[1], D. Brown[3], P. Oldiges[1], R. Robison[1], J. Arnold[1], N. Felix[1], S. Skordas[1], J. Gaudiello[1], T. Standaert[1], H. Jagannathan[1], D. Corliss[1], M.-H. Na[1], A. Knorr[3], T. Wu[1], D. Gupta[1], S. Lian[2], R. Divakaruni[1], T. Gow[1], C. Labelle[3], S. Lee[2], V. Paruchuri[1], H. Bu[1], and M. Khare[1]
IBM Research, 257 Fuller Road, Albany, NY 12203
[1]IBM, [2]Samsung Electronics, [3]GLOBALFOUNDRIES, email: njloubet@us.ibm.com

Si / SiGe





https://semiengineering.com/whats-after-finfets/

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2D Material landscape

- *Graphene*

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