THE FUTURE OF SEMICONDUCTOR
MOORE’S LAW PLUS

MARK PAPERMASTER
CTO & SVP, TECHNOLOGY & ENGINEERING
DEMAND FOR BETTER EXPERIENCES

Voice, Gesture & Face Recognition
Super High Resolution Displays
VR & AR
HUGE DEMAND FOR MORE COMPUTE

Big Data Analytics

High Performance Computing

Machine Learning
NEW APPROACH NEEDED - MOORE’S LAW HAS SLOWED

More Transistors
More Power Efficiency

Less Frequency Gain Per Node

40 YEARS OF MICROPROCESSOR TREND DATA

MOORE’S LAW **SLOWS** WHILE COSTS CONTINUE TO **INCREASE**

*Chart for Illustrative Purposes*
PROCESS TECHNOLOGY LEVERS TO **EXTEND** MOORE’S LAW

**CURRENT TECHNOLOGY**
- Trigate Devices
- Gate All Around
- Silicon
- Silicon Germanium
- Tunnel or Quantum Well
- III-V Materials

**NEW INTERCONNECT MATERIALS**
- Current Copper Interconnect
- New Interconnect Material

**NEXT GENERATION TRANSISTORS**
- EUV Lithography

**PROCESS TECHNOLOGY LEVERS**
- Integration

**INTEGRATION**
DIE SIZE INCREASES OVER TIME

MONOLITHIC VS. MULTICHIP

AMD EPYC Achieved 41% Die Cost Reduction

Hypothetical Monolithic

AMD EPYC Multichip Module
PACKAGING LEVERS TO EXTEND MOORE’S LAW

CHIPLETS & MULTI-CMOS PACKAGING

DIE STACKING & 2.5D INTEGRATION

INTERCONNECT DENSITIES

CHIPLETS
PACKAGES

System Optimizing Packaging

Min. bump pitch (um)
2020
2014
2020

HBM2 DRAM Die
HBM2 DRAM Die
HBM2 DRAM Die
HBM2 DRAM Die
Memory Controller
Interposer
Package Substrate
GPU

FLIP-CHIP
U-BUMPS/FAN-OUT
30um
55um
110um
180um

Optimizing Packaging
EXTENDING BEYOND THE SOC

Infinity Fabric is Architected to Efficiently Extend Beyond the SoC

One Protocol: On Die, Die-to-Die, and Socket-to-Socket

Flexible Multi-Die Solutions
MEMORY TECHNOLOGY TRENDS: COLLIDING FORCES

MEMORY DENSITY IMPROVEMENTS SLOWING

Average DRAM Density Increase/year


0% 10% 20% 30% 40% 50% 60% 70%

Driven by Data Analytics, Virtualization & Database

SERVER SYSTEM DRAM REQUIREMENTS

2012 2014 2016 2018 2020

0 GB 150 GB 300 GB 450 GB

Chart for Illustrative Purposes
Based on AMD Internal Data
TECHNOLOGY LEVERS FOR MEMORY & INTERCONNECT

NON-VOLATILE MEMORY
- Magnetic
- Phase Change
- Resistive

STACKED MEMORY
- Volatile
- Non-Volatile

PHOTONICS
- Discrete Transceivers
- Integrated Interface with Novel Fiber Alignment
- Improved Light Sources
MEMORY SYSTEM
DESIGN OPTIMIZATIONS

INTEGRATION ENABLES HIGHER BANDWIDTH AT LOWER POWER

<table>
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OPEN SOFTWARE SOLUTIONS FOR HETEROGENEOUS COMPUTE

Founding Member of Heterogeneous System Architecture Foundation

Radeon Open Compute (ROCm)
Support for x86, ARM® and POWER
Support for porting CUDA applications

Open Interconnect Standards for Heterogeneous Accelerators
ARCHITECTED TOGETHER TO DELIVER BREAKTHROUGH PERFORMANCE

DELIVERS ONE PETAFLOP IN A SINGLE RACK
NEW DESIGN APPROACHES...
HERE TO STAY

CHIPLETS & MULTICHIP MODULES
HETEROGENEOUS ACCELERATED COMPUTE
OPEN ECOSYSTEM
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