Energy Recovery and Recycling in Computation: Reversible Adiabatic Logic
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Motivation
- Power dissipation is the limiting factor for CMOS ICs.
- In standard CMOS the full energy of each bit is dissipated to heat at each logic transition.
- Adiabatic CMOS using reversible logic can dramatically reduce the power dissipation in a digital system.
- Landauer proposed that there is no lower limit on dissipation in computation. Dissipation must occur only when information is destroyed. This is known as the Landauer Principle. Is it correct?
- If the Landauer principle is correct, when would energy recovery make sense?
- An adiabatic microprocessor would make a significant circuit testbed for reversible adiabatic logic.
- Beyond-CMOS logic paradigms such as Quantum-dot Cellular Automata (QCA) map well onto reversible adiabatic logic.

When Does Energy Recovery Make Sense?
What if Power Density is Constrained?
Example $E_\infty = 1 \text{ aJ}$, $D_0 = 10 \text{ ps}$, $A_0 = 10^{-11} \text{ cm}^2$

\begin{itemize}
  \item Adiabatic: $E_{\text{EDA}} = E_{\infty} A_{\text{EDA}}$
  \item Multi-Core: $E_{\text{EDA}} = E_{\infty} A_{\text{EDA}}$
  \item Dark Si: $E_{\text{EDA}} = E_{\infty} A_{\text{EDA}}$
  \item Reversible: $E_{\text{EDA}} = E_{\infty} / C D_{A_0}$
\end{itemize}

Reversible adiabatic computing makes the best use of limited resources!

Minimum Energy for Computation
- Maxwell’s demon (1875) – by first measuring states, could perform reversible processes to lower entropy
- Szilard (1929), Brillouin (1962): measurement causes $k_B T \ln(2)$ dissipation per bit.
- Landauer (1961, 1970): only erasure of information must cause dissipation of $k_B T \ln(2)$ per bit
  \textbf{(Landauer’s Principle)}
- Bennett (1982): full computation can be done without erasure.
  
  logical reversibility – physical reversibility

Still somewhat controversial.

Adiabatic CMOS with Bennett Clocking
Reversible computation always has some associated overhead
Bennett Clocking (retractile cascade) combined with split-level logic can implement with minimum spatial overhead.

Design Tools
- Design tools based on SystemVerilog and Mentor Graphics ModelSim for Bennett clocked adiabatic circuits
- Ramp Logic Timing simulation
- Standard Cell Library
- Bennett Energization Sequence Checker
- Standard Logic Synthesis

Cell Design

Cell Initial Experimental results

Test of the Landauer Principle
Room temperature operations on a 73 k\textsuperscript{0}T bit of information

Copy 0
Copy 1
Erase 1
Erase 0

Measured dissipation was 0.005 k\textsuperscript{0}T (15 yJ).

MIPS Microprocessor
Three Bennett zones of 12 phases, no pipelining
Reduced instruction set, but still universal
32 bit instructions, 8 bit data path
From Weste and Harris (Addison-Wesley)

Fabricated Chip
Notre Dame 1\textmu m process
Mosis fab in process
Approximately 5700 transistor, 45% in adiabatic circuits.

References

CONCLUSIONS
- There is no fundamental lower limit of energy!
- Reversible computation can recover signal energy and avoid dissipation to heat.
- Design tools were developed to support the design of Bennett-clock ed adiabatic circuits.
- A reduced MIPS microprocessor was designed in adiabatic logic.
- Paradigms such as QCA can avoid limits due to leakage.