ITRS ERD Workshop Summary

"Bridging the research gap between emerging architectures and devices"
Workshop dates: February 26-27, 2015
Summary by Erik DeBenedictis

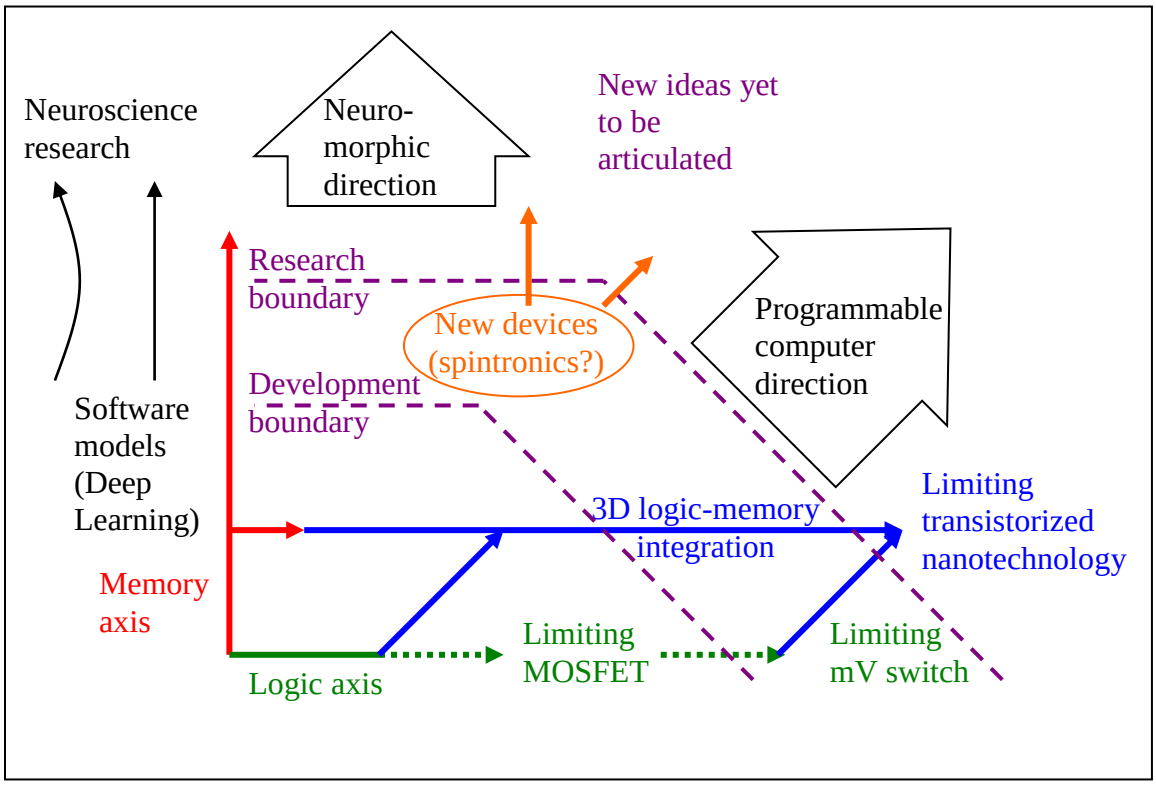
ITRS held a workshop on Emerging Research Devices at Stanford University February 26-27, co-sponsored by IEEE Rebooting Computing. Leadership of both organizations was present. The workshop agenda is at the end. .

This document will attempt to organize a diverse group of talks. The diagram below will be used as an organizational framework.

Categorization of approaches

The majority of the talks supported one of two ultimate directions for computation: programmable and neuromorphic.

- Programmable computation: DeBenedictis, Williams, Koike, Nikonov, Badaroglu, Yablonovich
- Neuromorphic computation: Arthur, Srinivasa, Roy, Burr, Bourianoff, Franzon
- Devices for either of above: Marinella, Kang, Fujita, Das
- Other approaches: Shanbhag (statistical), Niemier (waves), Naeemi (spin interconnect)



Programmable computation

The future of programmable computing will involve a merger of logic and memory/storage into a 3D technology platform. There are questions about the replacement of the transistor and options for the memory. Most options for memory will be non-volatile, hence making memory into storage. At a high level, this merger is represented by the red and green lines in the diagram merging into blue, which proceeds off the right side to "limiting transistorized nanotechnology" (although the memory devices are usually not transistors).

Badaroglu gave a presentation on the current ITRS roadmap, essentially the green line along the bottom of the diagram. In order to maintain Moore's Law, a series of technologies will need to be introduced on a schedule. This talk was on logic, and the technologies extended to negative capacitance transistors and TFETs at the end of the roadmap.

Yablanovich gave a talk on issues for the TFET, concluding that increased attention would be needed for "interface traps." TFETs comprise the second segment of the green line ending in "limiting mV switch."

Nikonov spoke on comparative benchmarking of CMOS replacements. Different transistor variants were compared in terms of power and speed. This corresponded to detailing the green line in the diagram by comparing 10 versions of the approach.

Devices that are made in 2D can usually be packaged in 3D, which was a basis for talks by DeBenedictis and Williams – corresponding to the blue arrows on the diagram. DeBenedictis gave a long term scaling rule for 3D at constant power. Williams spoke of an HP R&D project called "The Machine" set to produce a computer exploiting non-volatile 3D storage in 1-2 years.

Koike's talk was on FPGA architecture issues for power control. The FlexPower method was a way of applying more power to devices on the critical path and less elsewhere.

Neuromorphic computation

In contrast to programming on conventional computers, neuromorphic computers can learn and thereby replace both a programmable computer and its programmer. The upwards pointing arrow labeled "neuromorphic direction" in the diagram above highlights the difference from the "programmable computer direction." Neuromorphic computing is also associated with neuroscience research and software such as Deep Learning. These latter two are drawn outside the main axis in the diagram above because they are outside the scope of this meeting.

Talks on neuromorphic computation included outbriefs by DARPA Synapse program performers IBM and HRL. IBM described their TrueNorth system, which is a very complex 28 nm CMOS implementation of a spiking neuromorphic system. TrueNorth uses offline learning, which is different from the others below.

HRL described their Synapse product, which was spiking and based on memristors. The circuit included a memristor for state but surrounded by transistors that generated spikes.

Roy proposed a neuromorphic system based on analog magnetic synapses. New devices are illustrated in the diagram in orange, generally bypassing existing roadmaps, logic/memory separation, and jumping directly to the application.

Burr described a phase-change-memory (PCM)-based system. This analysis applied to either crossbar or fully isolated transistors, and concluded there are noise variance properties in analog devices like PCM or RRAM (memristors) that need to be considered in neuromorphic operation.

Bourianoff spoke on neural computing based on coupled oscillators. He illustrated this with a video of mechanical musical metronomes coupling in phase due to sharing a weakly secured base. The implementation discussed was coupled spin-torque oscillators.

Franzon presented various properties of neural systems relevant to neuromorphic computing.

Devices

In prior ITRS roadmaps, ERD produced a chapter with sections on logic devices and memory devices, followed by shorter sections on architecture, "More than Moore," etc. In the diagram, these correspond to the red memory axis and the green logic axis. Marinella and Das were editors of the memory and logic sections in past years, and they summarized last year's sections.

Kang presented the value of evolutionary developments in memory from a business perspective. For example new memory increases cache sizes, thus enabling new products.

Fujita spoke about a spintronic implementation (spin-torque transfer) of MRAM.

Nikonov and Young compared speed and power for logic using CMOS-type devices in a manner that was cross compatible with Spintronics. This appears on the diagram in orange, with Nikonov's analysis based on logic gates (as opposed to neurons) that would correspond to programmable computers.

Other

Shanbhag presented random and statistical computing. Any logic device can be considered to have Boolean properties of computation but also a probability of error. Computers traditionally assume a low component error rate, with errors leading to a computer system failure. The end of a roadmap is defined as the point where error become problematic. The new approach would consider errors a normal part of operation, to which mitigations like error detection and correction would be applied.

Niemier gave a talk on wave-based computations. Optical lenses can be characterized as computing Fourier transforms. The same principle applies to propagating waves in other media, such as Spintronic systems. Extremely complex waveguides can be constructed that generalize the single algorithm of a Fourier transform.

Neemi spoke on spintronic wave propagation. Spintronic logic creates waves where domain inversions mark the transition from one Boolean level to another. The motion of these domain inversions could become the basis for a type of new computation.

ITRS/IEEE RC Emerging Research Devices Meeting Agenda, Stanford University

Feb. 26, Thursday

Time	Presentation Title	Speaker	Affiliation
8:45 AM	Overview of Emerging Research Memory Devices	Matt Marinella	Sandia/ERD
9:15 AM	Emerging Memories: Harvesting Values from System Perspectives	Seung Kang	Qualcomm
10:00 AM	Processor in Memory and Storage	Erik DeBenedictis	Sandia/ERD
11:00 AM	"The Machine"	Stan Williams	HP
11:45 AM	FPGA Development with Emerging Research Devices	Hanpei Koike	AIST
1:15 PM	Normally-off Computing (Nonvolatile Memory Computing) using Advanced STT-MRAM	Shinobu Fujita	Toshiba
2:00 PM	Overview of Emerging Research Logic Devices	Shamik Das	MITRE/ERD
2:30 PM	Benchmarking of Beyond-CMOS Devices and Circuits	Dmitri Nikonov	Intel
3:30 PM	IBM TrueNorth: Architecture, Technology, and Ecosystems	John Arthur	IBM
4:15 PM	Neuromorphic Architectures for Energy Efficient Processing	Narayan Srinivasa	HRL
5:00 PM	Efficient Neural Computing using Cellular Array of Magneto-Metallic Neurons	Kaushik Roy	Purdue
5:45 PM	Non-volatile Memory as a Neuromorphic Synapse: Effect of imperfections	Geoff Burr	IBM/ERD

Feb. 27, Friday

8:15 AM	More Moore scaling: opportunities and inflection points	Mustafa Badaroglu	Qualcomm
8:45 AM	Statistical information processing: Computing on Nanoscale Fabrics	Naresh Shanbhag Andrew Singer, Philip Wong	UIUC Stanford
10:15 AM	Spintronics for Beyond-CMOS Computing	Ian Young, Dmitri Nikonov	Intel
12:15 AM	Non-Boolean computing based on spatial temporal wave excitation and emerging transistor technologies	Mike Niemer, Wolfgang Porod	U. Notre Dame
1:15 PM	Computational Nanofabrics based on coupled oscillators	George Bourianoff	Intel
2:15 PM	The Challenge of a New Low-Voltage Switch That is Much More Sensitive Than the Transistor	Eli Yablonovitch	UC Berkeley
3:00 PM	Energetics at the End of the Roadmap and Cognitive Computing	Paul Franzon	NCSU
4:00 PM	Interconnects for Beyond-CMOS Devices: Challenges and Opportunities	Azad Naeemi	Georgia Tech