2nd IEEE Rebooting Computing Summit
May 14-16, 2014
The Chaminade Resort & Spa, Santa Cruz, CA

The second Rebooting Computing Summit (RCS 2) is a gathering of experts and leaders from industry, academia, and government to lay out paradigms and milestones for achieving the vision defined in the first Rebooting Computing Summit held on Dec. 11-13, 2013 in Washington, DC (http://rebootingcomputing.ieee.org/RCS1.pdf). RCS 2 will focus on the following approaches that may be implemented in next-generation computing systems:

- Augmentation of CMOS
- Neuromorphic Computing
- Approximate Computing
- Adiabatic/Reversible Computing

The **final RCS 2 agenda** includes introductory presentations on each of these approaches by corresponding experts, breakout group discussions addressing milestones and plans for each approach, and concluding summaries from each working group. In addition, a collaboration has been initiated for this effort between the International Technology Roadmap for Semiconductors (ITRS, http://www.itrs.net) and the IEEE Rebooting Computing initiative.

Some discussions about these RCS 2 topics and related issues are being posted on the RC Blog http://rebootingcomputing-ieee.blogspot.com/
Please feel free to join the conversation about the future of computing!

Augmentation of CMOS
Silicon CMOS circuits have been the central technology of the digital revolution, and the performance of CMOS devices and systems have been following Moore's law (doubling in performance every year or two) for the past several decades, together with scaling to smaller dimensions and larger scale integration. CMOS appears to be reaching physical limits, including size and power density, but there is presently no technology available that can take its place. How should CMOS be augmented with integration of new materials, devices, logic, and system design, in order to extend enhancement of computer performance for the next decade or more? And how should these new technologies be coordinated with the semiconductor industry roadmap (ITRS)? For further information, see "Moore's Law: The First Ending and a New Beginning", http://rebootingcomputing.ieee.org/images/files/images/pdf/mooreslaw.pdf.

Neuromorphic Computing
The brain is a computer constructed from slow, non-uniform, unreliable devices on the 10 ï?m scale, yet its computational performance exceeds that of the best supercomputers in many respects, with much lower power dissipation. What does this have to teach us about the next generation of electronic computers? Neuromorphic computing studies the organization of neurons and interconnecting synapses to identify those features (such as massive device-level parallelism, adaptive circuitry, and content-

addressable memory) that may be emulated in electronic circuits, and attempts to construct a new class of computers that combines the best features of both electronics and brains.

For further information see http://en.wikipedia.org/wiki/Neuromorphic_engineering, also "Thinking in Silicon" http://www.technologyreview.com/featuredstory/522476/thinking-in-silicon/.

Another recent extensive review of the field is "Finding a Roadmap to Achieve Large Neuromorphic Hardware Systems", by Jennifer Hasler and Bo Marr, available online at http://journal.frontiersin.org/Journal/10.3389/fnins.2013.00118/full.

Approximate Computing

Historically computing hardware and software were designed for numerical calculations requiring a high degree of precision, such as 32 bits. But many present applications (such as image processing and data mining) do not require an exact answer; they just need a sufficiently good answer quickly. Furthermore, conventional logic circuits are highly sensitive to bit errors, which are to be avoided at all cost. But as devices get smaller and their counts get larger, the likelihood of random errors increases. Approximate computing represents a variety of approaches that seek to trade off accuracy for speed, efficiency, and error-tolerance.

For further information, see "EnerJ, the Language of Good-Enough Computing" http://spectrum.ieee.org/computing/software/enerj-the-language-of-goodenough-computing, also "Approximate Computing: A New Paradigm for Energy-Efficient Design" http://rebootingcomputing.ieee.org/images/files/images/pdf/6569370.pdf.

Adiabatic/Reversible Computing

One of the primary sources of power dissipation in digital circuits is associated with switching of transistors and other elements. The basic binary switching energy is typically far larger than the fundamental limit ~kBT, and much of the energy is effectively wasted. Adiabatic and reversible computing describe a class of approaches to reducing power dissipation on the circuit level by minimizing and reusing switching energy, and applying supply voltages only when necessary.

For further information, see http://en.wikipedia.org/wiki/Adiabatic_circuit, also "Adiabatic Technique for Energy-Efficient Circuit Design" http://rebootingcomputing.ieee.org/images/files/images/pdf/adiabatic.pdf